Appl. No. 10/697,289; Filed: Oct 31, 2003
Dkt No. 1875.4360005; Group Unit: 2819
Inventors: CATALASAN et al.
Tel. No.: 202-371-2600
For: Coupling of Signals Between Adjacent Functional Blocks in an Integrated Circuit Chip

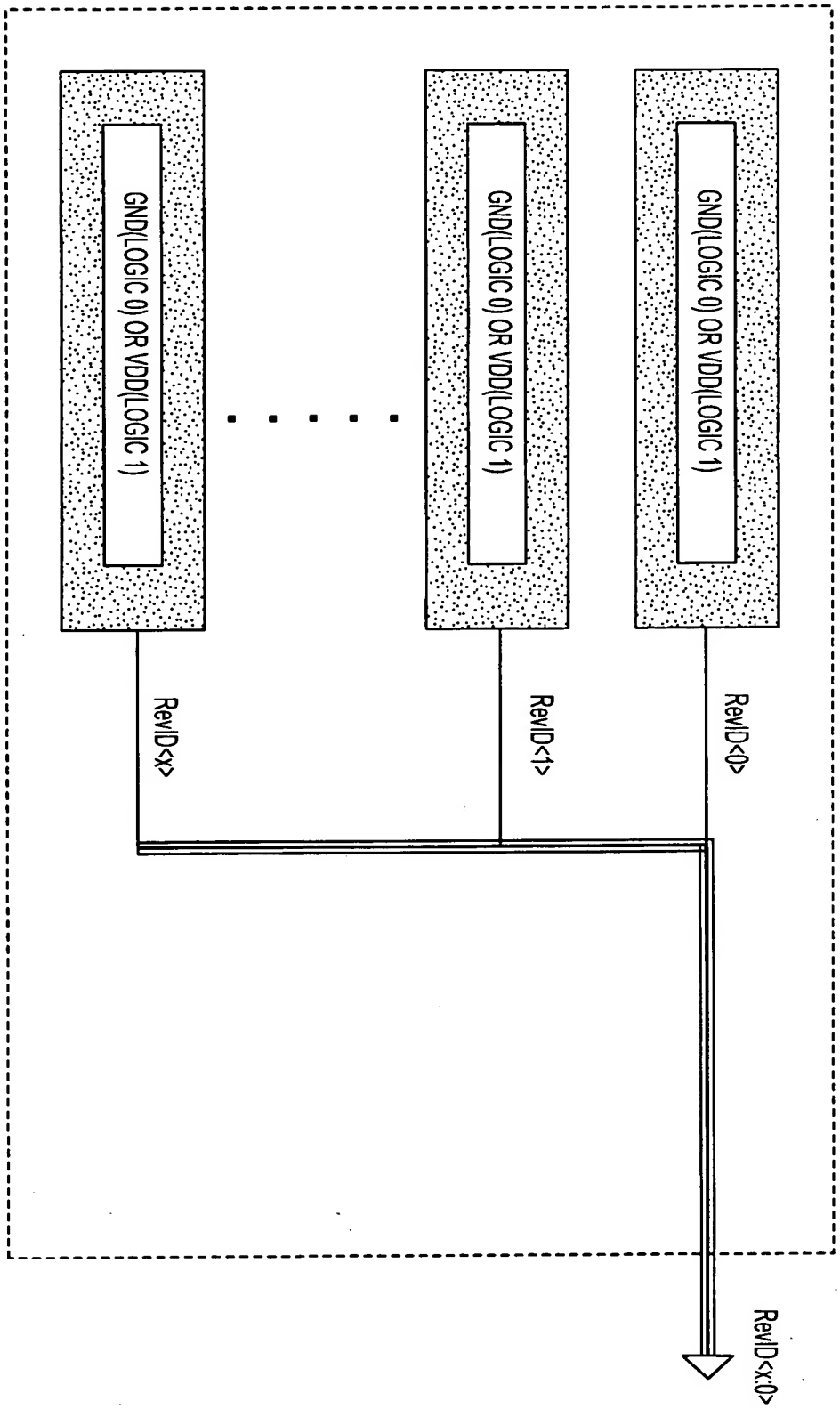


FIG. 1

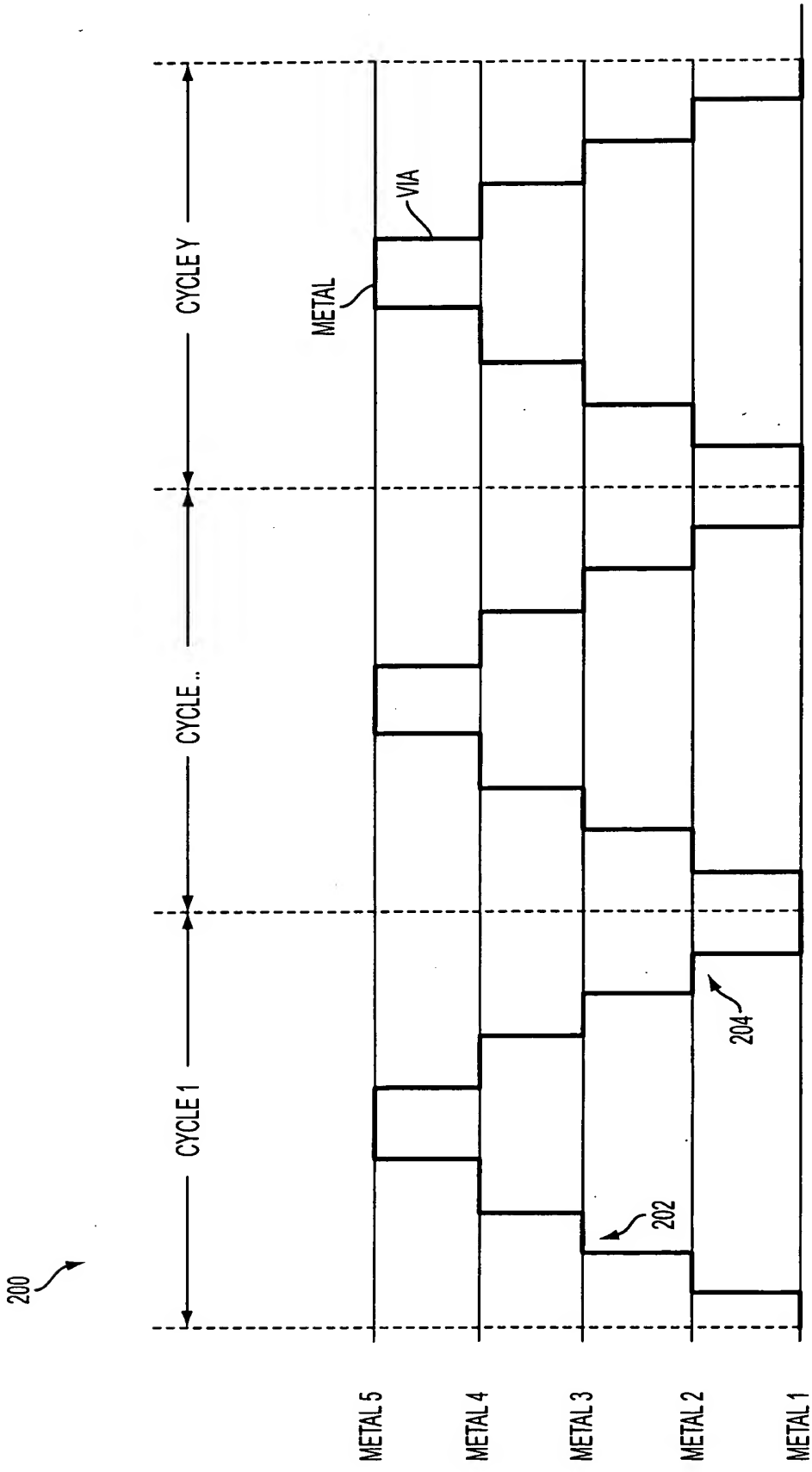

200
CYCLE 1
CYCLE ..
CYCLE Y
METAL
VIA
202
204
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 2

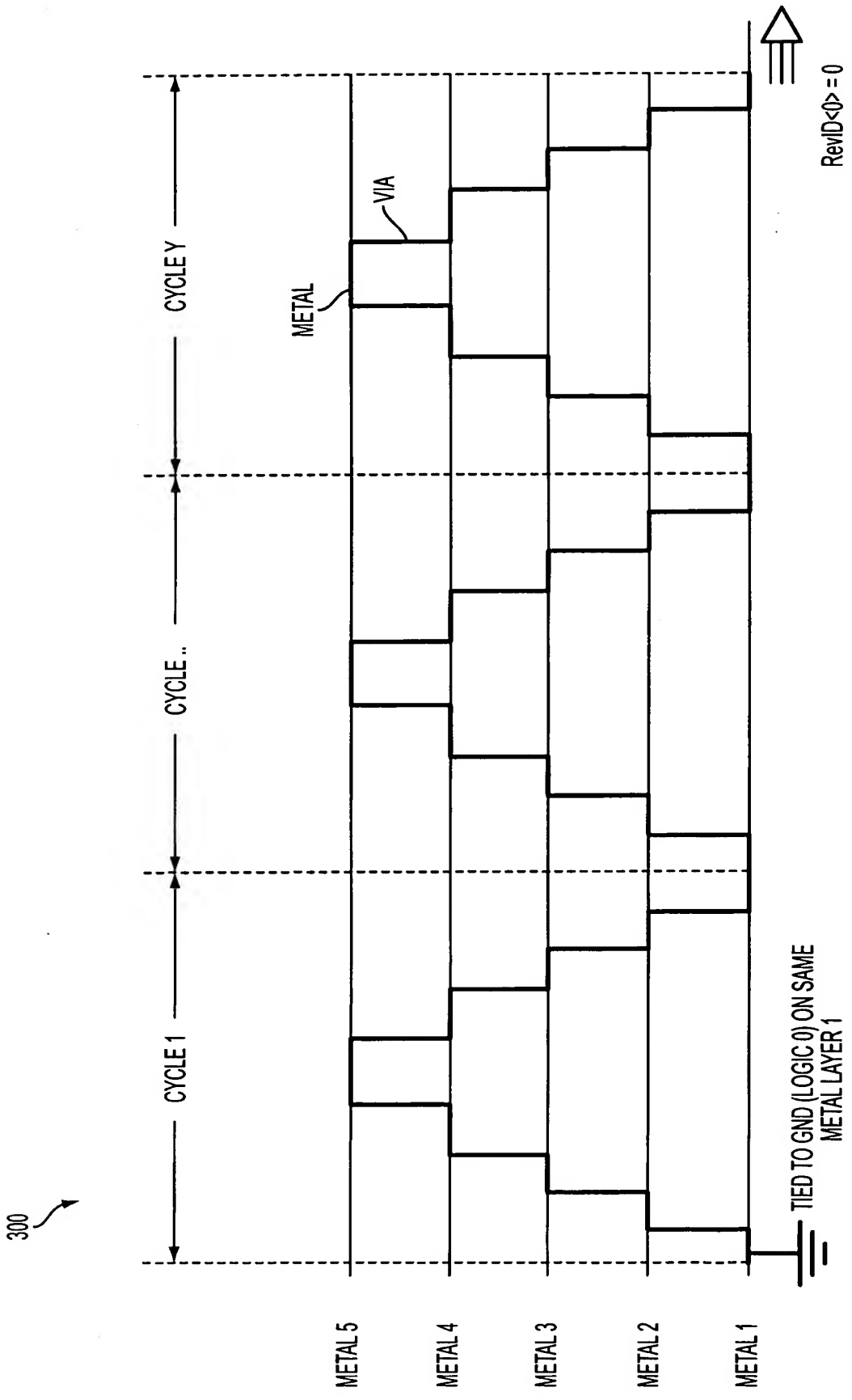

300
CYCLE 1
CYCLE ..
CYCLE Y
METAL
VIA
RevID<0> = 0
TIED TO GND (LOGIC 0) ON SAME METAL LAYER 1
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 3A

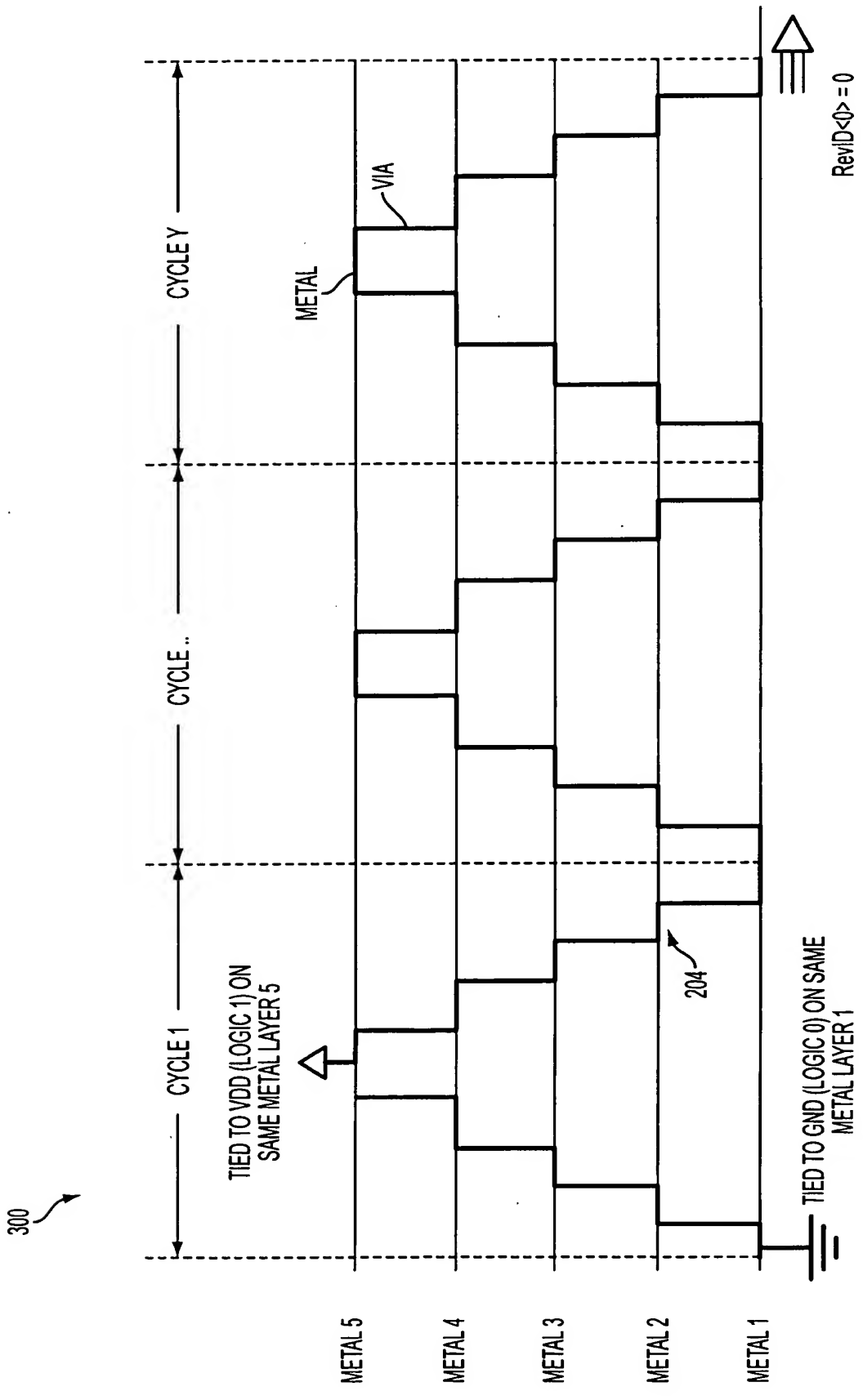

300
CYCLE 1
CYCLE ..
CYCLE Y
TIED TO VDD (LOGIC 1) ON SAME METAL LAYER 5
METAL
VIA
204
TIED TO GND (LOGIC 0) ON SAME METAL LAYER 1
RevID<0> = 0
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 3B

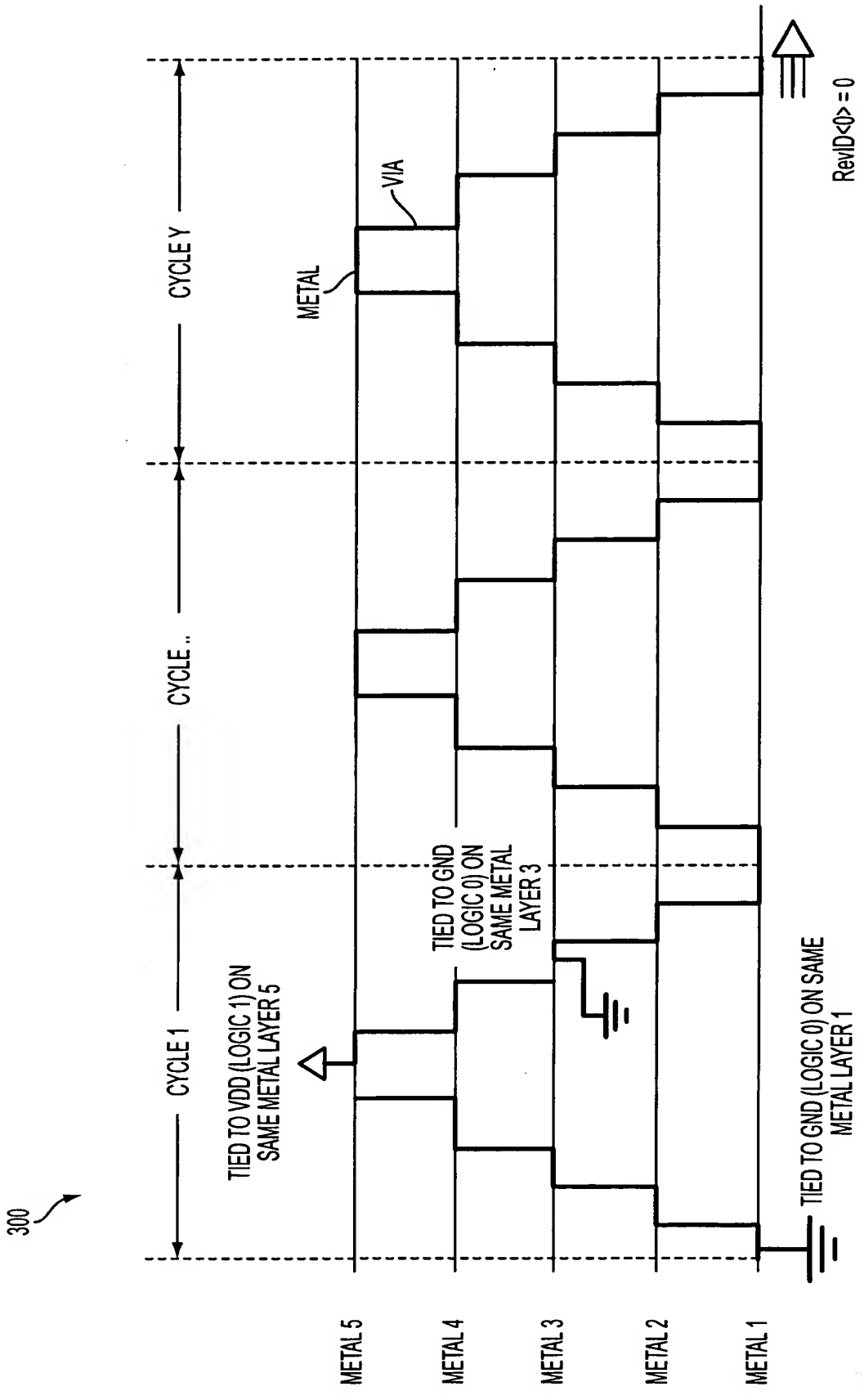

300
CYCLE 1
CYCLE ..
CYCLE Y
TIED TO VDD (LOGIC 1) ON SAME METAL LAYER 5
TIED TO GND (LOGIC 0) ON SAME METAL LAYER 3
TIED TO GND (LOGIC 0) ON SAME METAL LAYER 1
METAL
VIA
RevID<0> = 0
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 3C

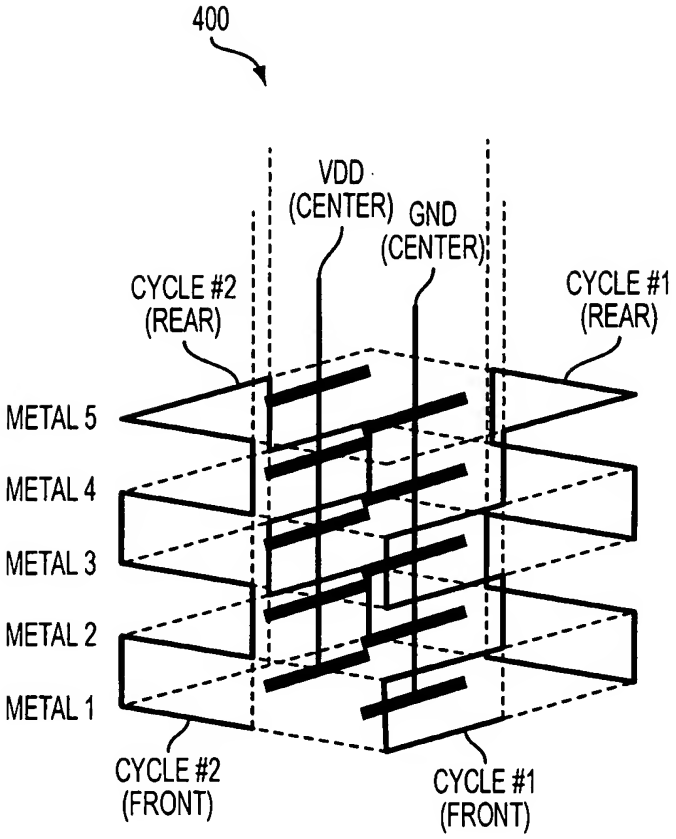

400
VDD
(CENTER)
GND
(CENTER)
CYCLE #2
(REAR)
CYCLE #1
(REAR)
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1
CYCLE #2
(FRONT)
CYCLE #1
(FRONT)

FIG. 4

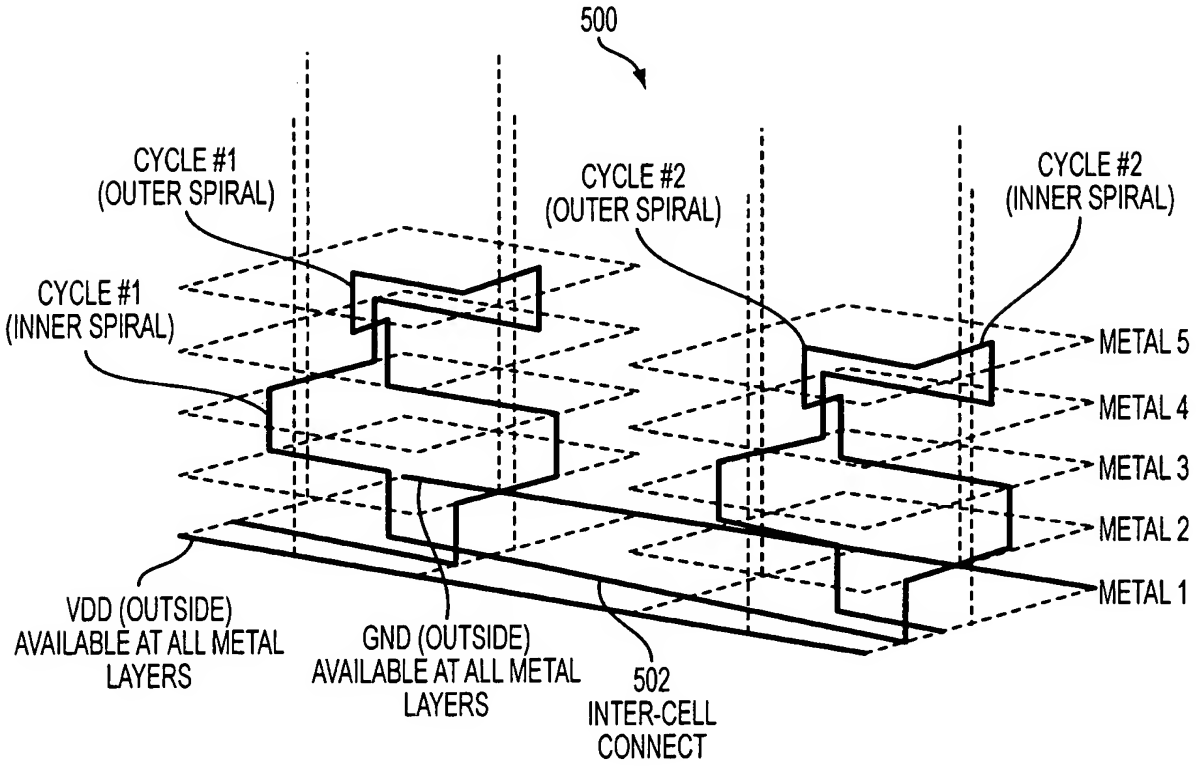

500
CYCLE #1
(OUTER SPIRAL)
CYCLE #2
(OUTER SPIRAL)
CYCLE #2
(INNER SPIRAL)
CYCLE #1
(INNER SPIRAL)
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1
VDD (OUTSIDE)
AVAILABLE AT ALL METAL
LAYERS
GND (OUTSIDE)
AVAILABLE AT ALL METAL
LAYERS
502
INTER-CELL
CONNECT

FIG. 5A

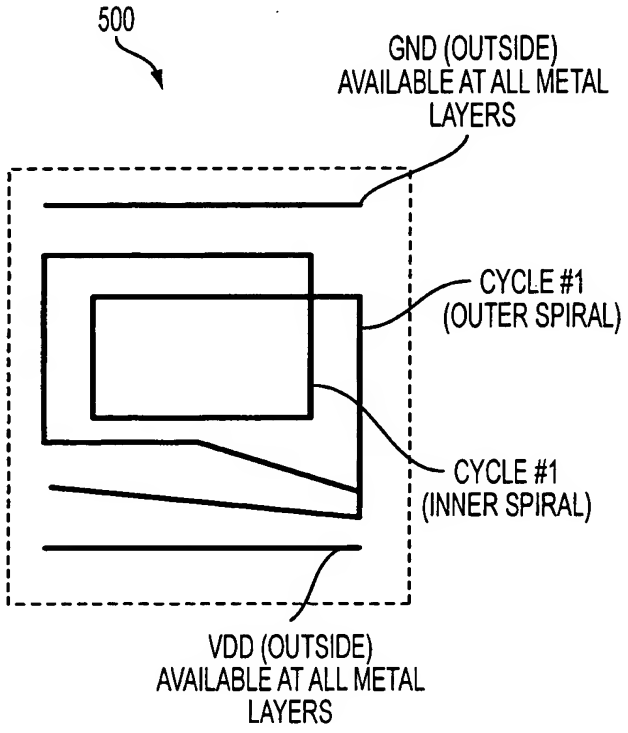

500
GND (OUTSIDE)
AVAILABLE AT ALL METAL
LAYERS
CYCLE #1
(OUTER SPIRAL)
CYCLE #1
(INNER SPIRAL)
VDD (OUTSIDE)
AVAILABLE AT ALL METAL
LAYERS

FIG. 5B

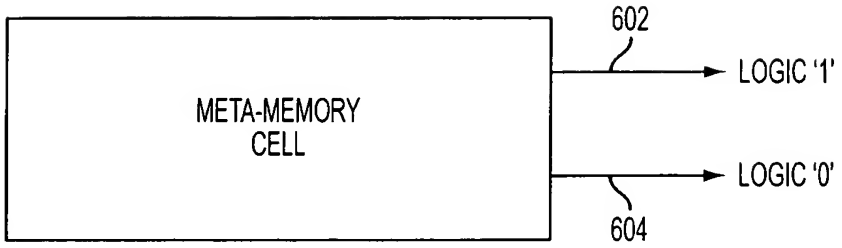


FIG. 6

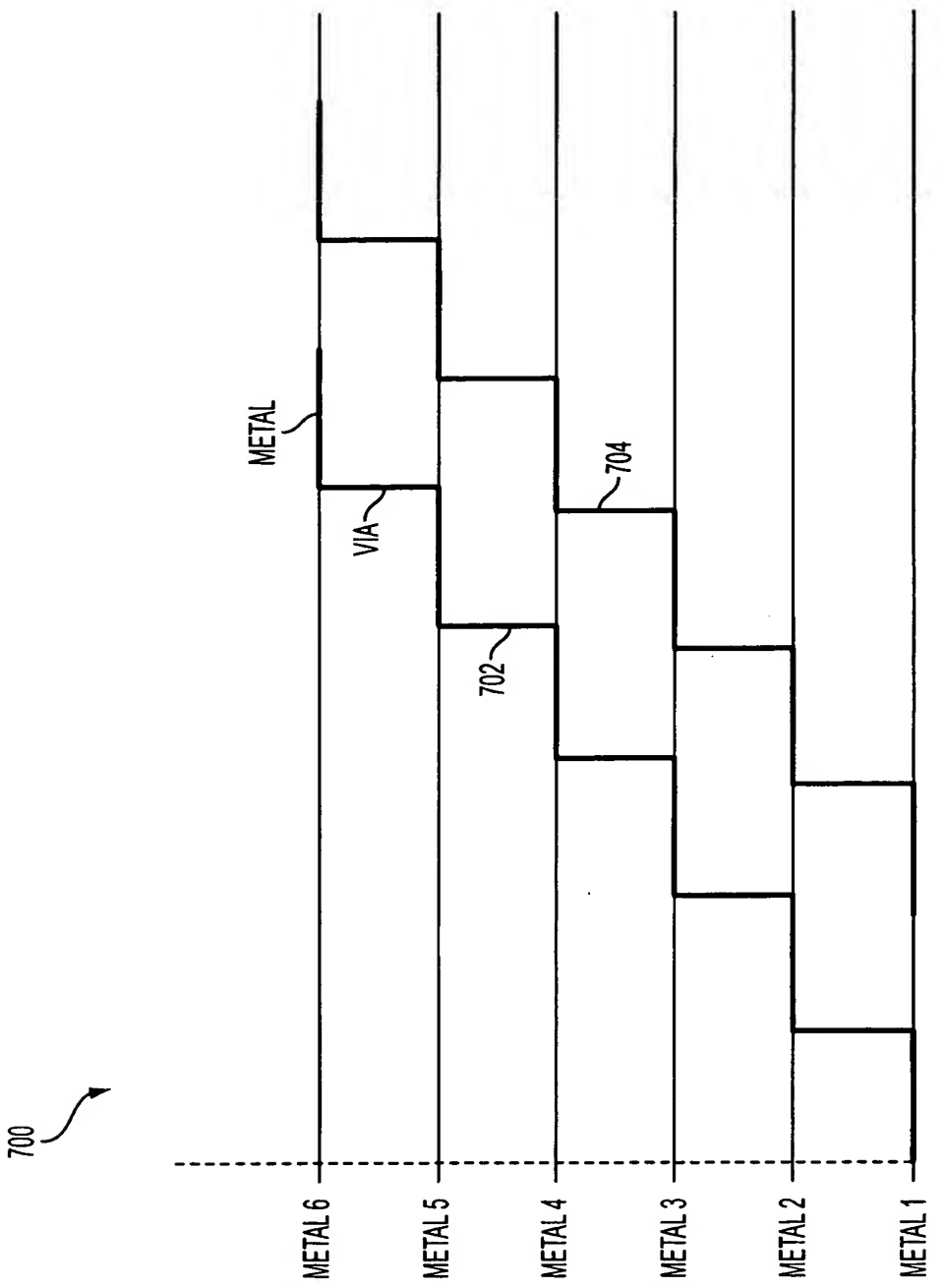

700
METAL
VIA
702
704
METAL 6
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 7A

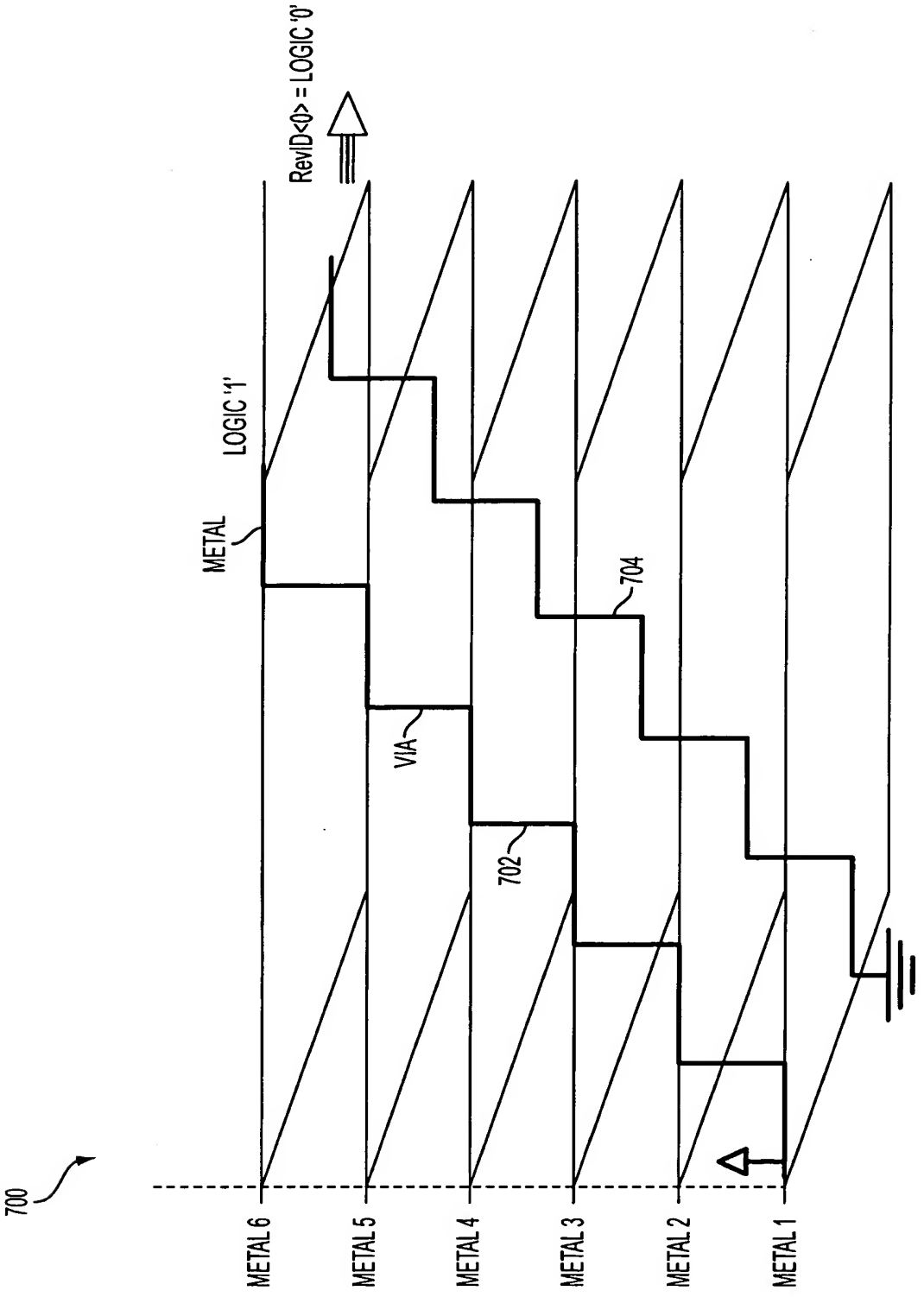

RevID<0> = LOGIC '0'
LOGIC '1'
METAL
VIA
702
704
700
METAL 6
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 7B

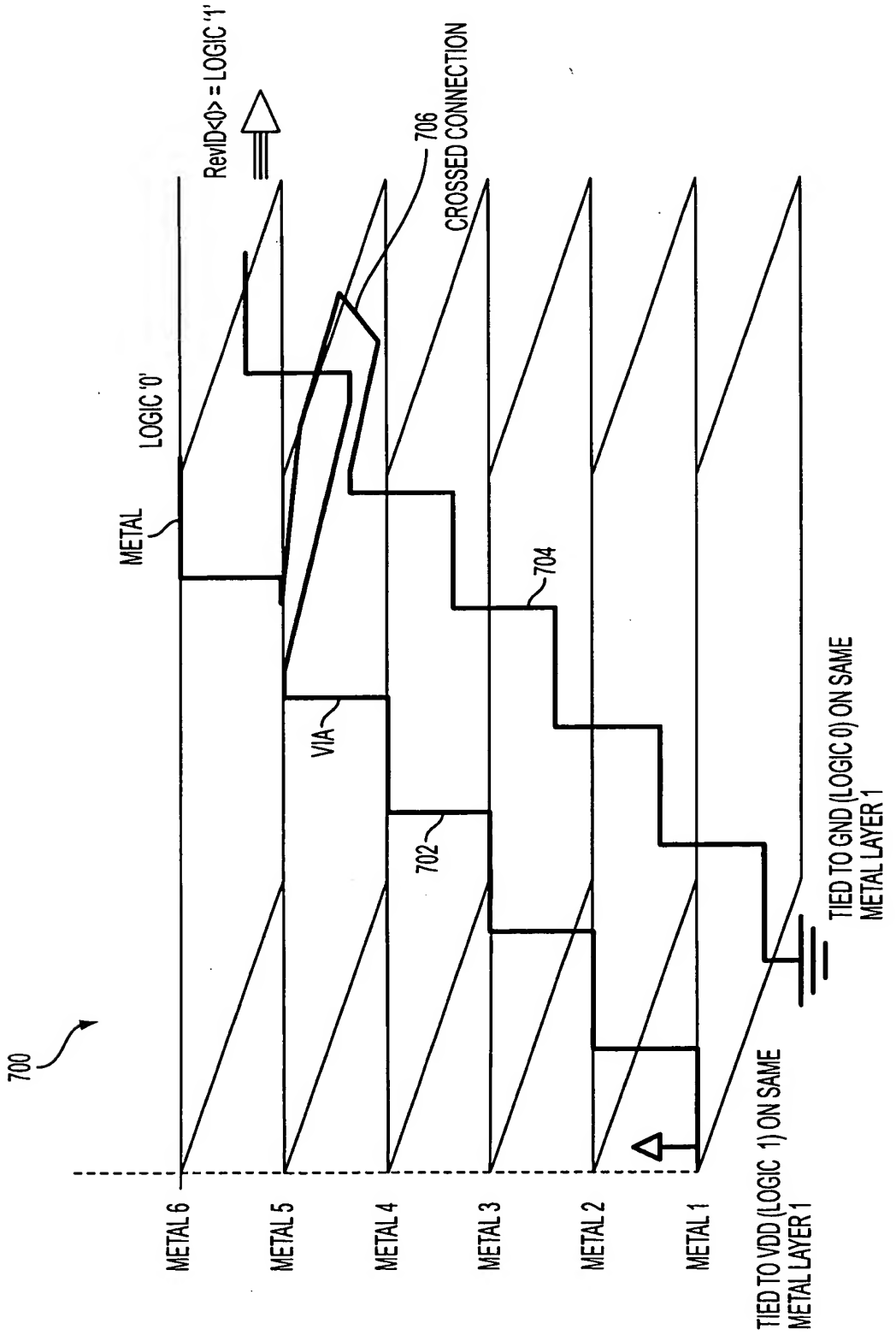

700
RevID<0> = LOGIC '1'
706
CROSSED CONNECTION
LOGIC '0'
METAL
704
VIA
702
TIED TO GND (LOGIC 0) ON SAME METAL LAYER 1
TIED TO VDD (LOGIC 1) ON SAME METAL LAYER 1
METAL 6
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 7C

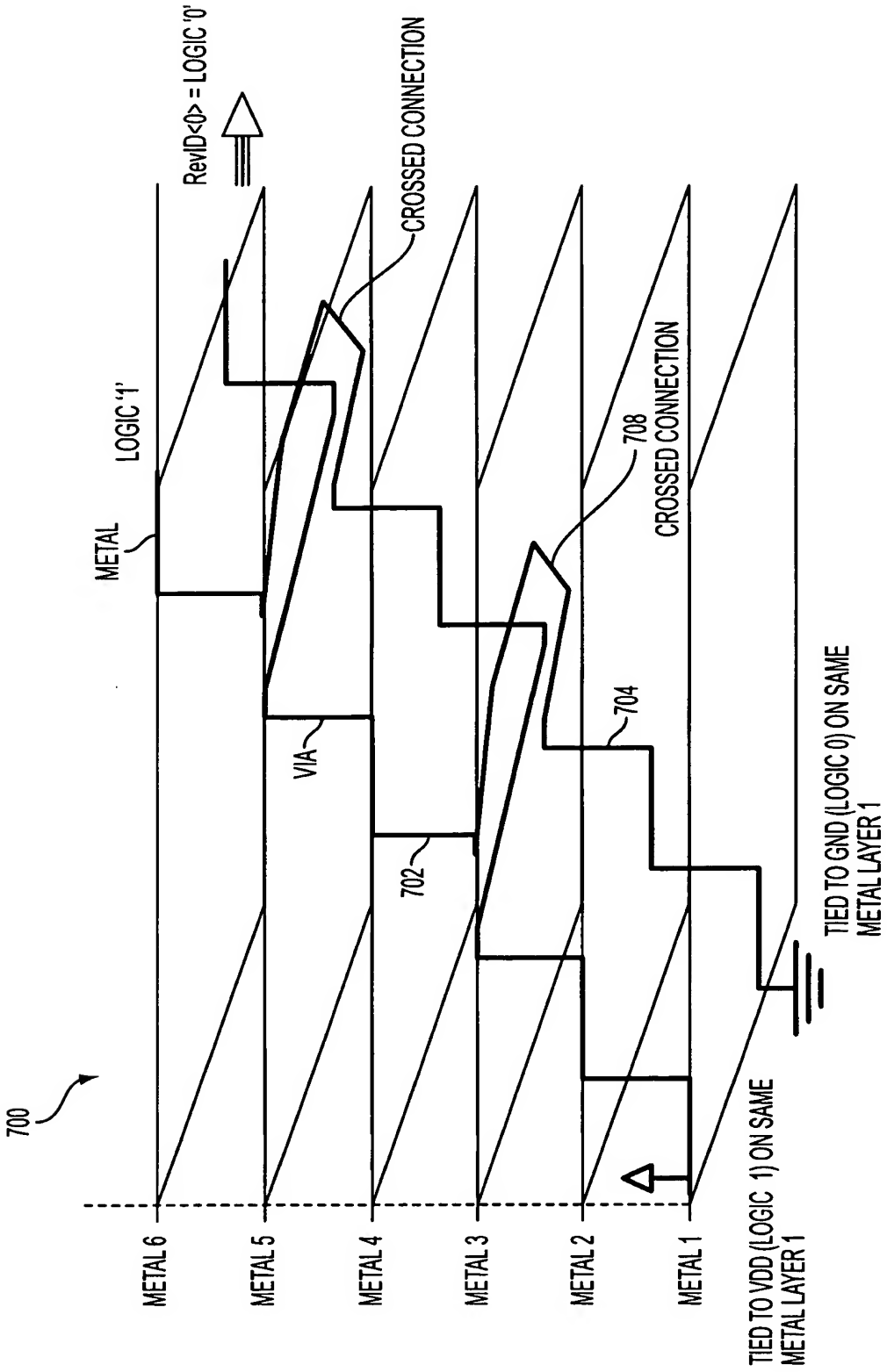

700
METAL 6
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1
TIED TO VDD (LOGIC 1) ON SAME METAL LAYER 1
TIED TO GND (LOGIC 0) ON SAME METAL LAYER 1
VIA
702
704
708
CROSSED CONNECTION
CROSSED CONNECTION
METAL
LOGIC '1'
RevID<0> = LOGIC '0'

FIG. 7D

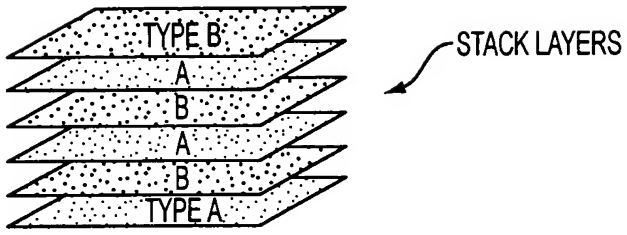

TYPE B
A
B
A
B
TYPE A
STACK LAYERS

FIG. 8A

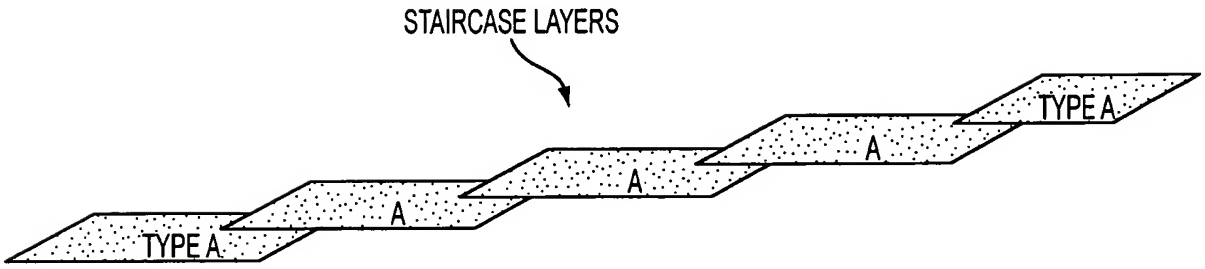

STAIRCASE LAYERS
TYPE A
A
A
A
TYPE A

FIG. 8B


A_IN
B_IN
METAL/VIA LAYER
A_OUT
B_OUT

FIG. 9A

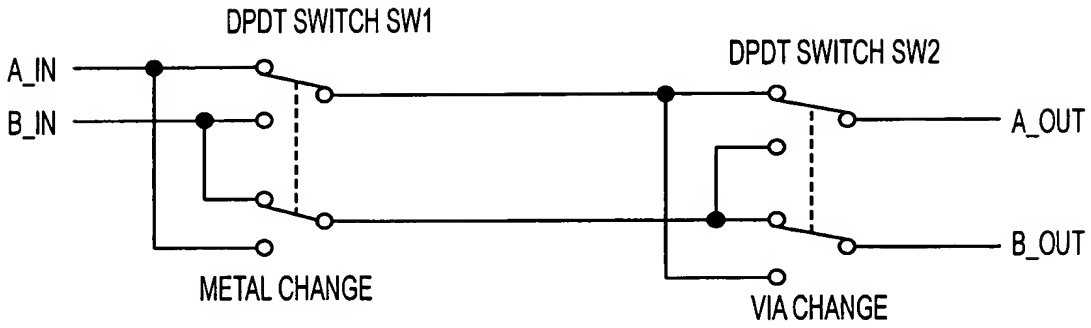

DPDT SWITCH SW1
DPDT SWITCH SW2
A_IN
B_IN
A_OUT
B_OUT
METAL CHANGE
VIA CHANGE

FIG. 9B

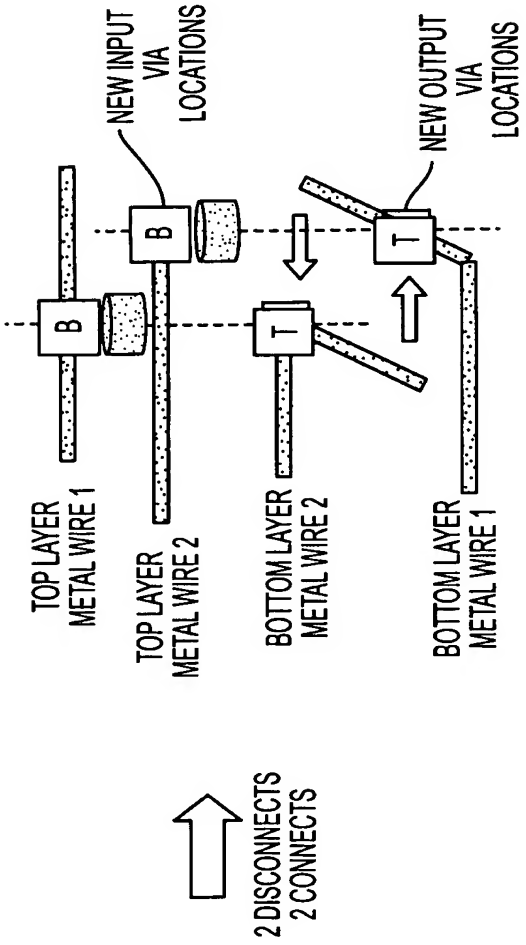

NEW INPUT VIA LOCATIONS
NEW OUTPUT VIA LOCATIONS
B
T
TOP LAYER METAL WIRE 1
TOP LAYER METAL WIRE 2
BOTTOM LAYER METAL WIRE 2
BOTTOM LAYER METAL WIRE 1
2 DISCONNECTS
2 CONNECTS

FIG. 9D

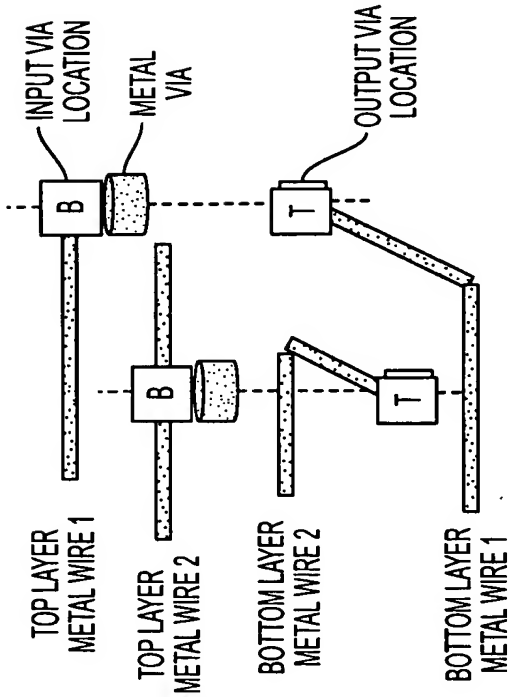

INPUT VIA LOCATION
METAL VIA
OUTPUT VIA LOCATION
B
T
TOP LAYER METAL WIRE 1
TOP LAYER METAL WIRE 2
BOTTOM LAYER METAL WIRE 2
BOTTOM LAYER METAL WIRE 1

FIG. 9C

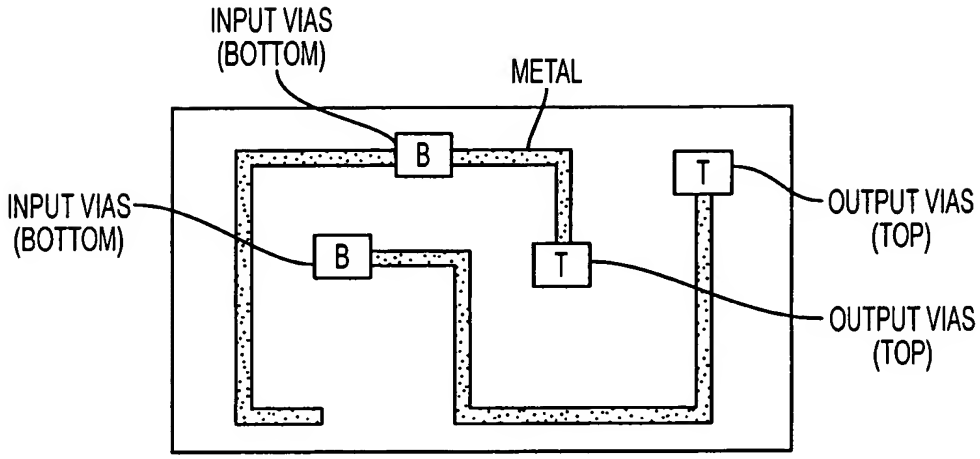


FIG. 10A

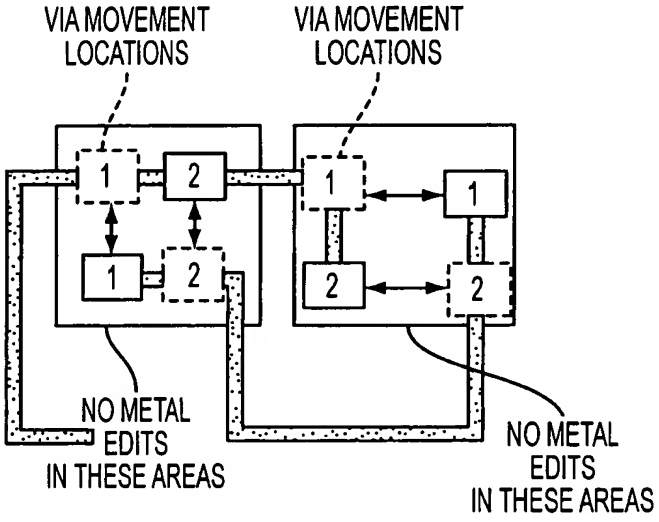


FIG. 10B

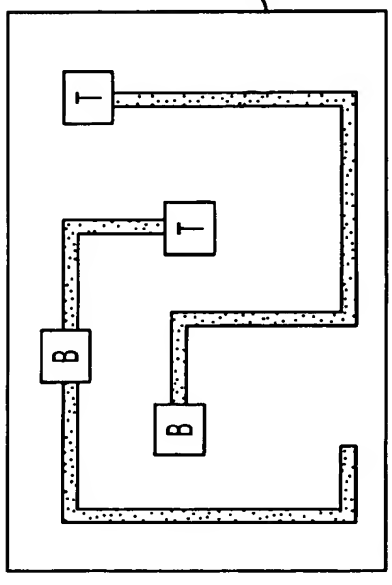


FIG. 11A

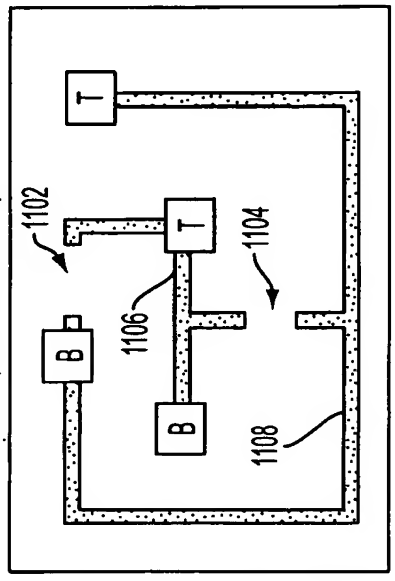


FIG. 11B

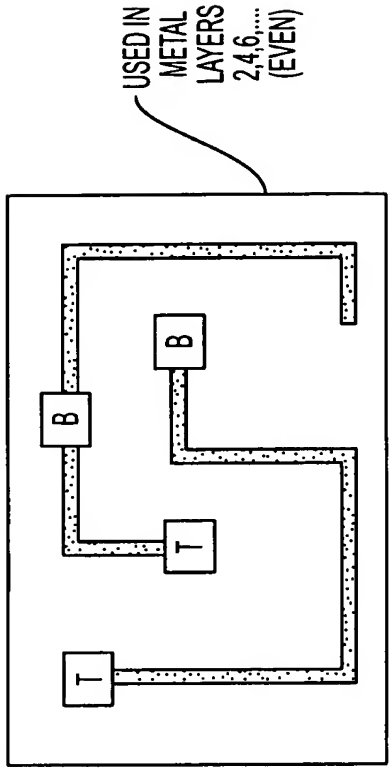


FIG. 11C

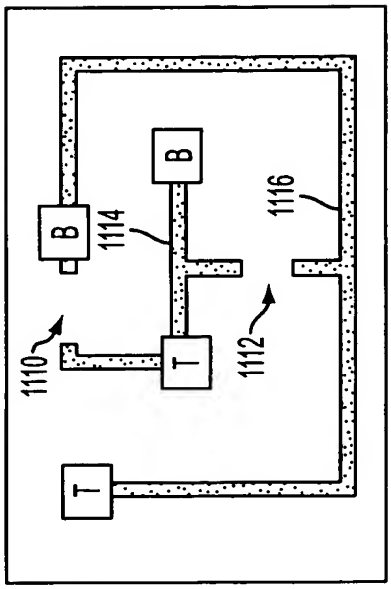
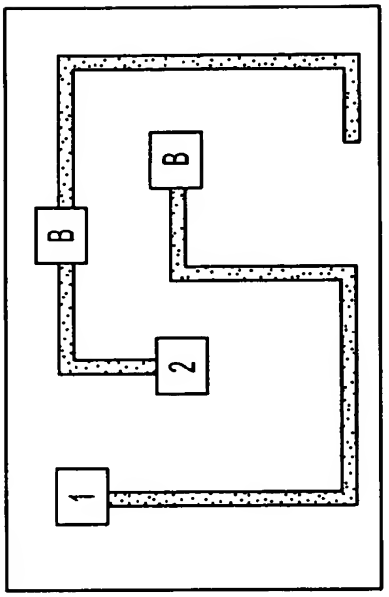


FIG. 11D



FLIP BASIC PATTERN

TO FIG. 12D

FIG. 12C

FROM FIG. 12C

FLIP BASIC PATTERN W/VIA CHANGE
(2 DISCONNECTS, 2 CONNECTS)

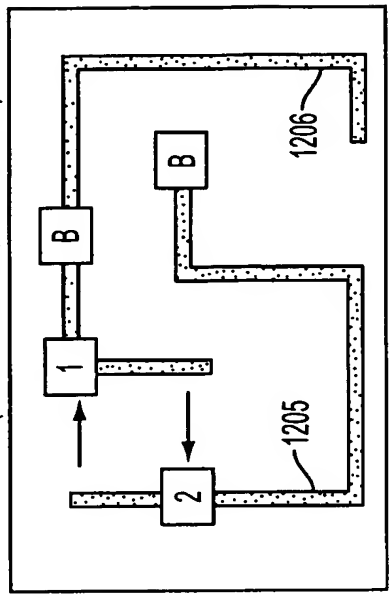
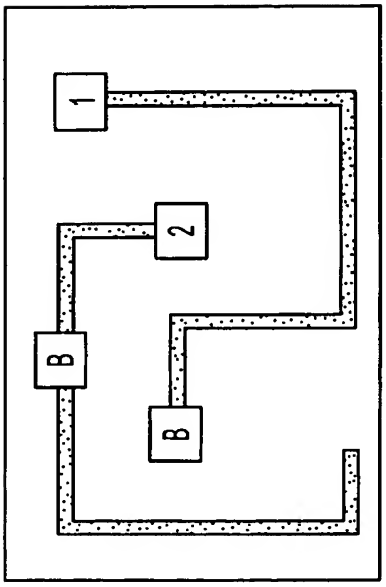


FIG. 12D



BASIC PATTERN

TO FIG. 12B

FIG. 12A

FROM FIG. 12A

BASIC PATTERN W/VIA CHANGE
(2 DISCONNECTS, 2 CONNECTS)

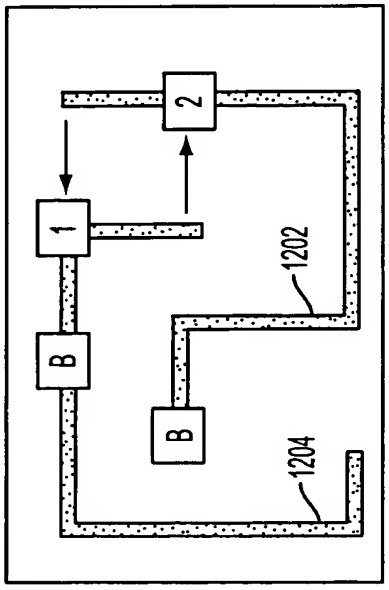


FIG. 12B

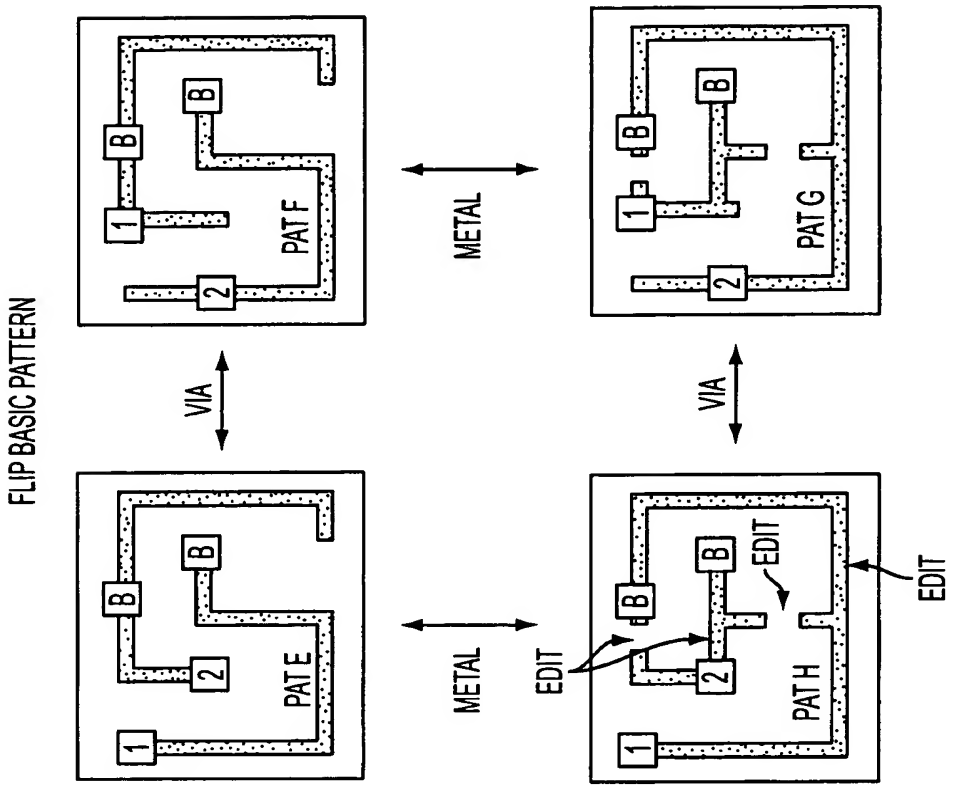

FLIP BASIC PATTERN
VIA
VIA
METAL
METAL
PAT F
PAT G
PAT E
PAT H
EDIT
EDIT
EDIT
B
1
2

FIG. 14

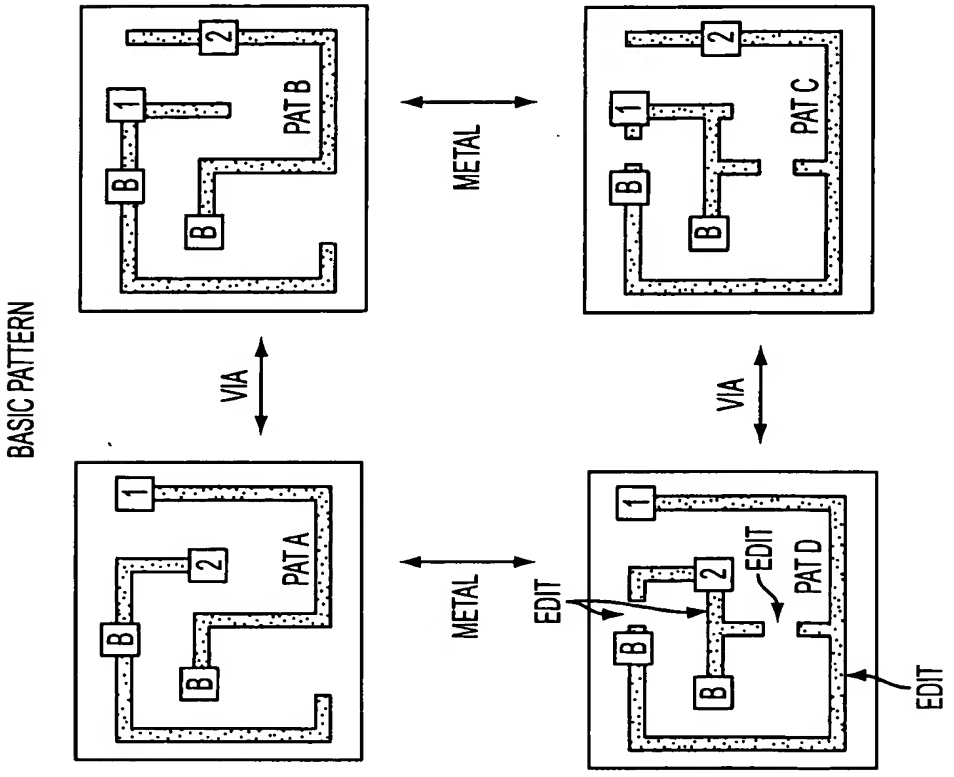

BASIC PATTERN
VIA
VIA
METAL
METAL
PAT A
PAT B
PAT C
PAT D
EDIT
EDIT
EDIT
B
1
2

FIG. 13

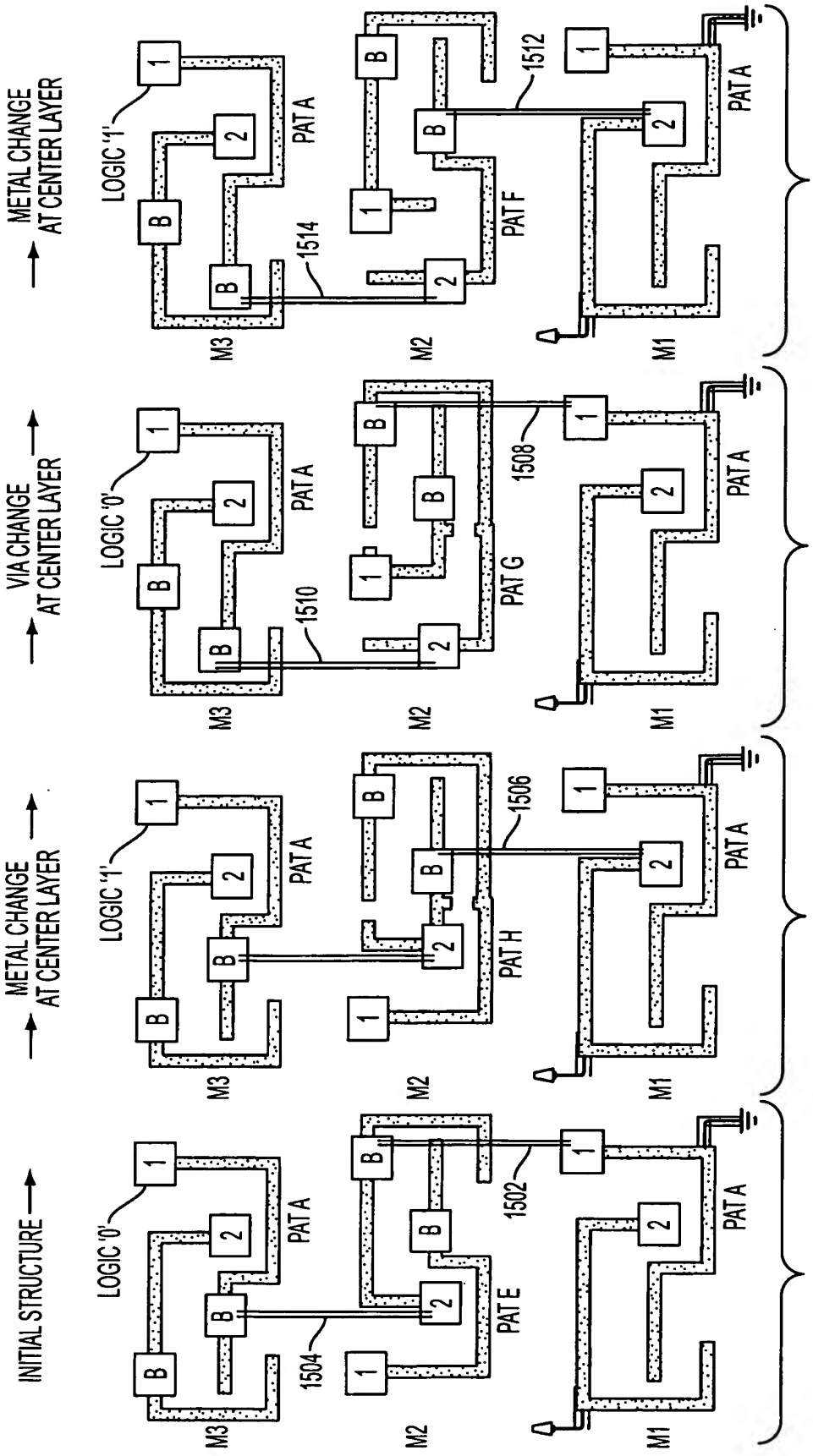


FIG. 15A

FIG. 15B

FIG. 15C

FIG. 15D

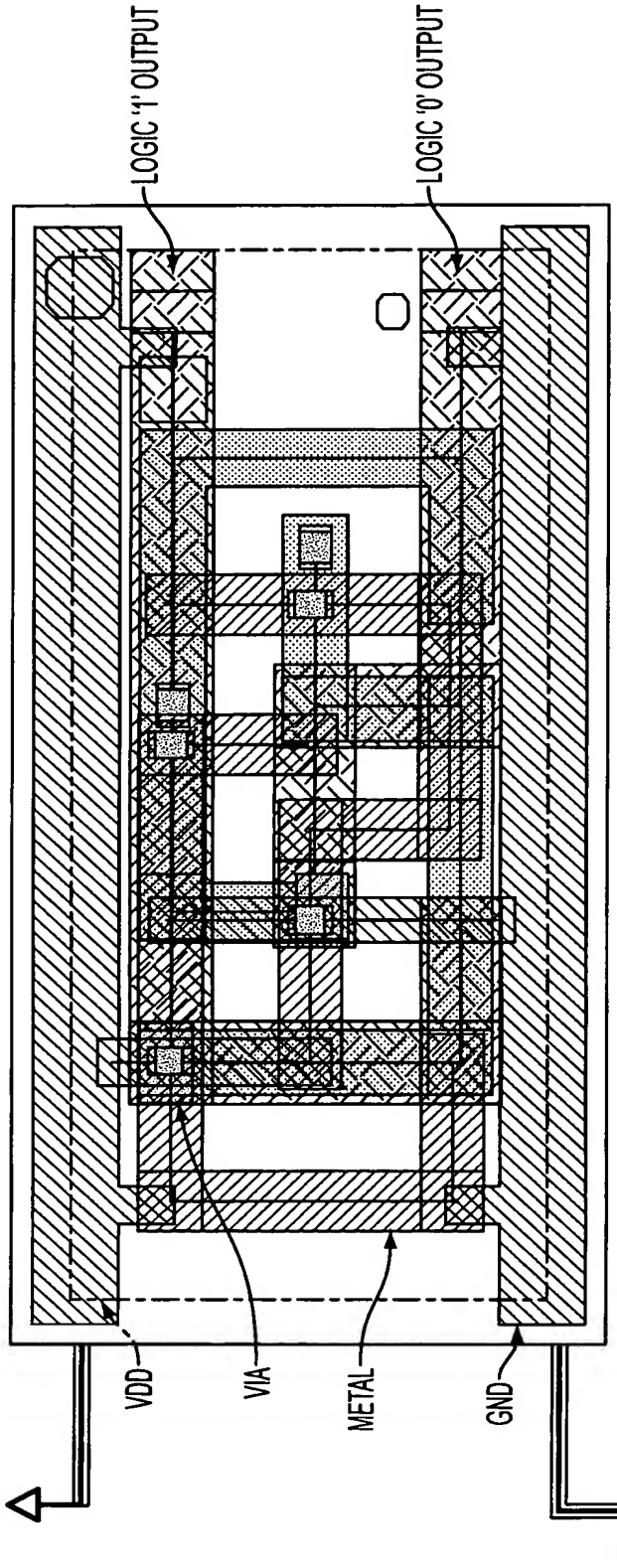


FIG. 16

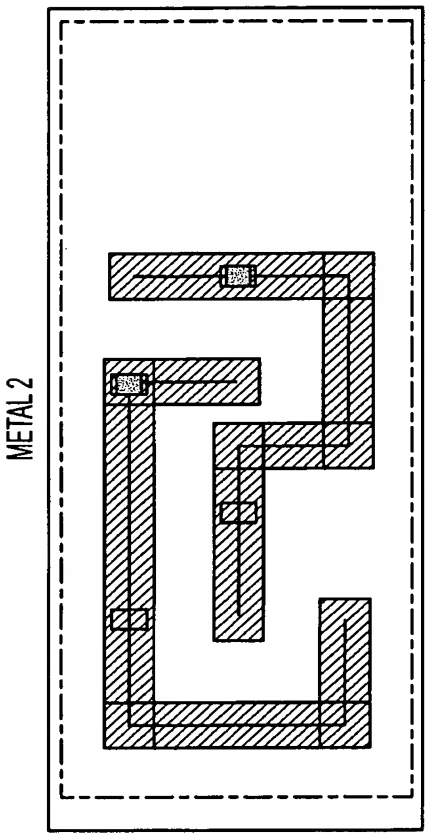


FIG. 17B

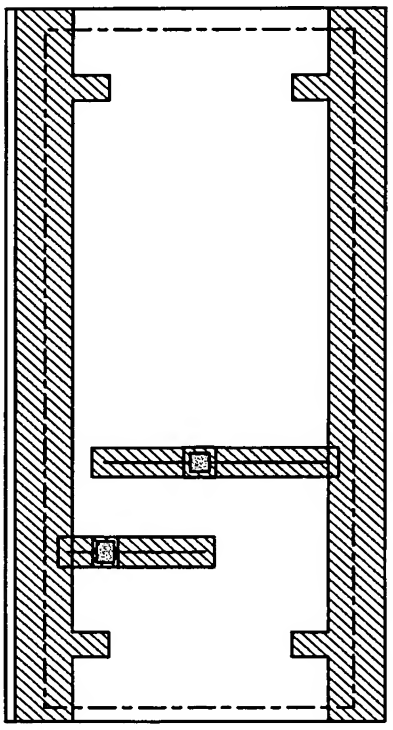


FIG. 17A

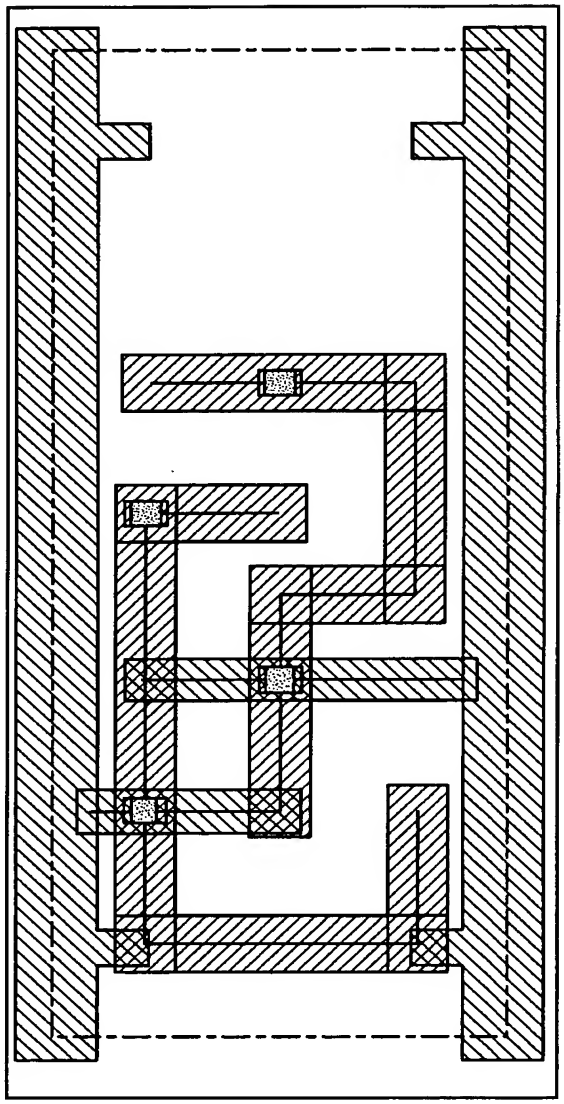


FIG. 17C

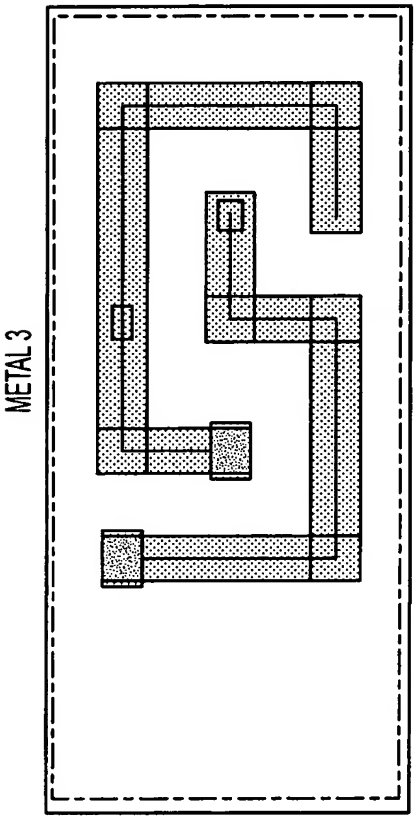


FIG. 18B

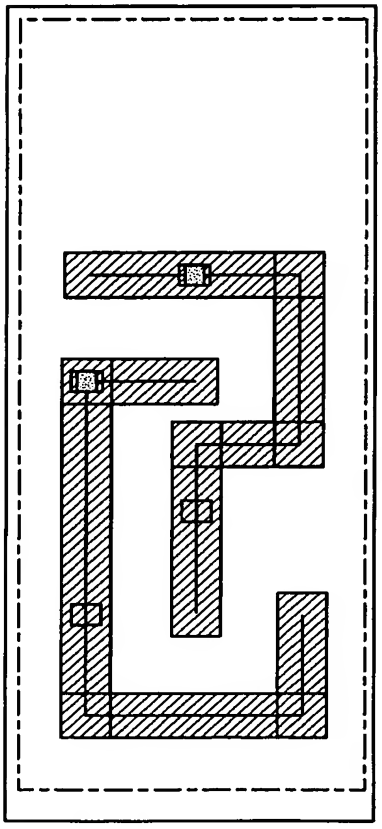


FIG. 18A

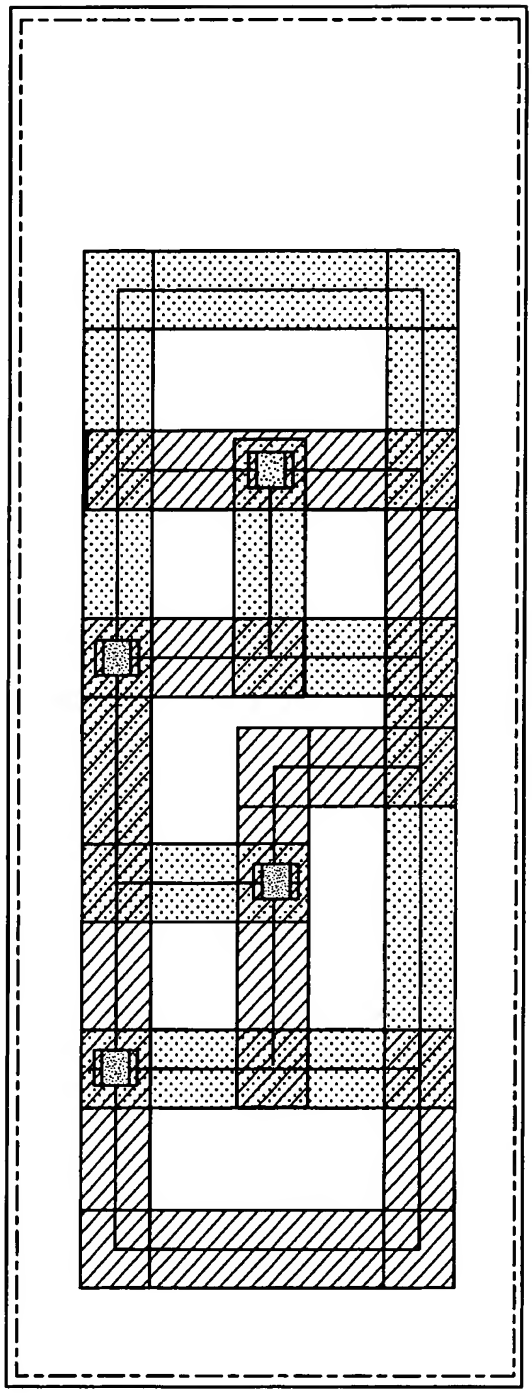


FIG. 18C

Appl. No. 10/697,289; Filed: Oct 31, 2003
Dkt No. 1875.4360005; Group Unit: 2819
Inventors: CATALASAN et al.
Tel. No.: 202-371-2600
For: Coupling of Signals Between Adjacent Functional Blocks in an Integrated Circuit Chip

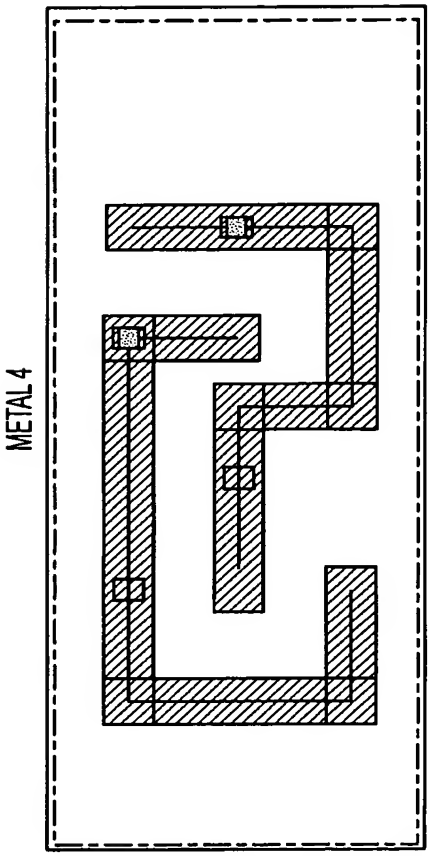


FIG. 19B

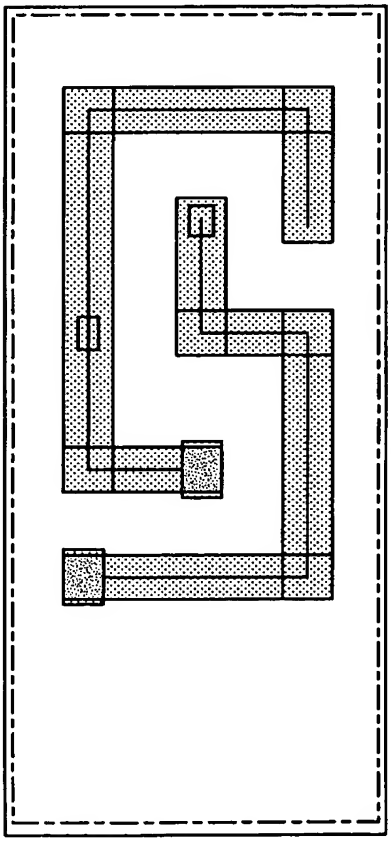


FIG. 19A

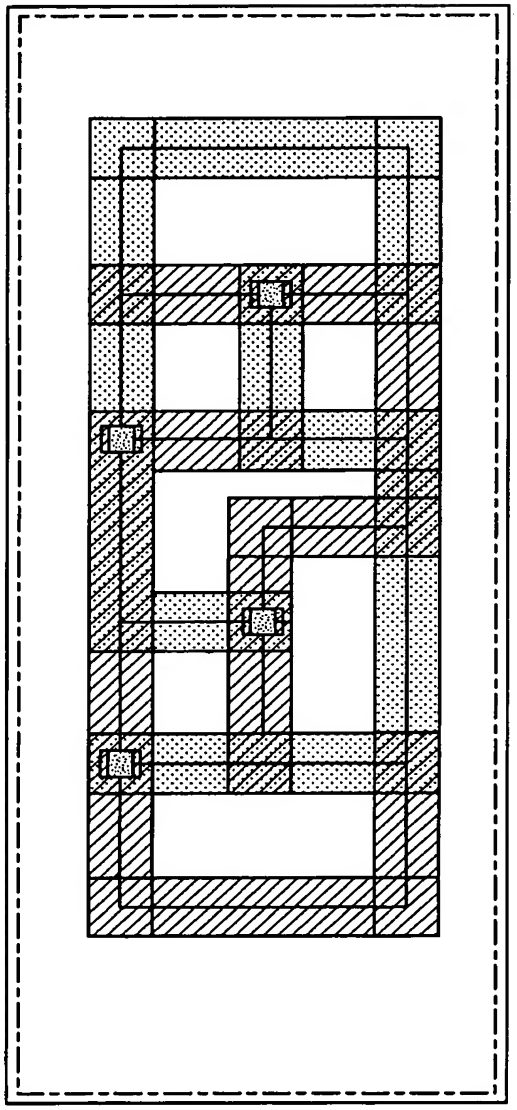


FIG. 19C

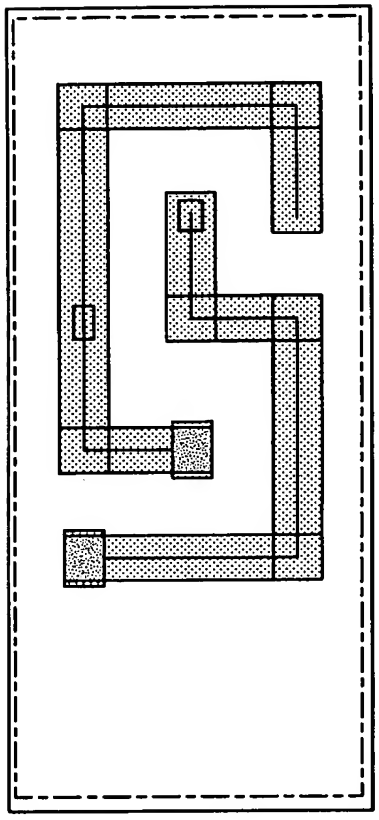


FIG. 20B

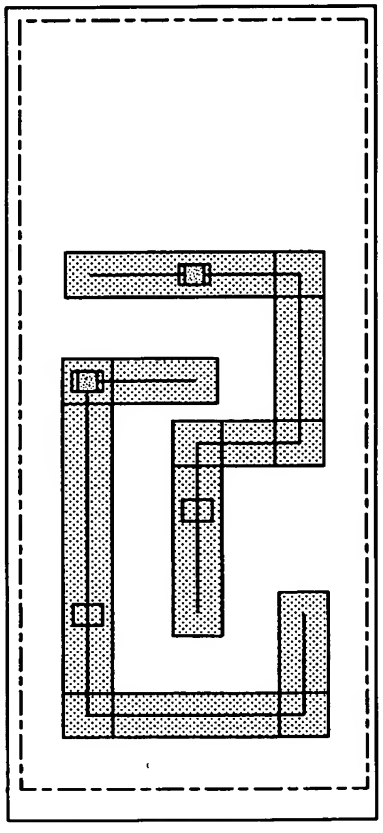


FIG. 20A

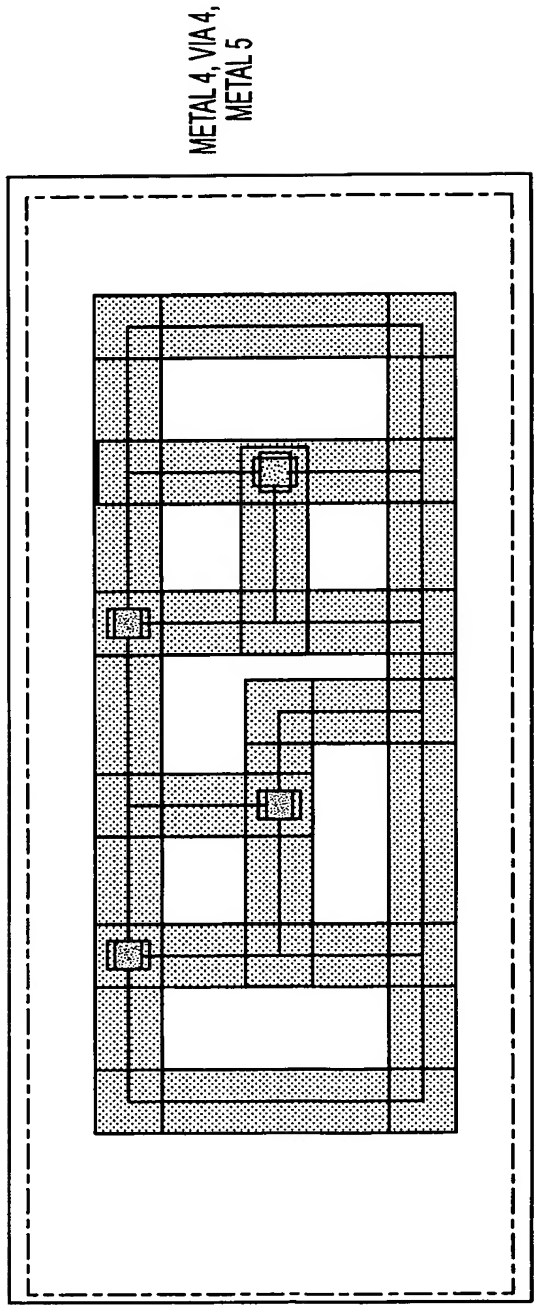


FIG. 20C

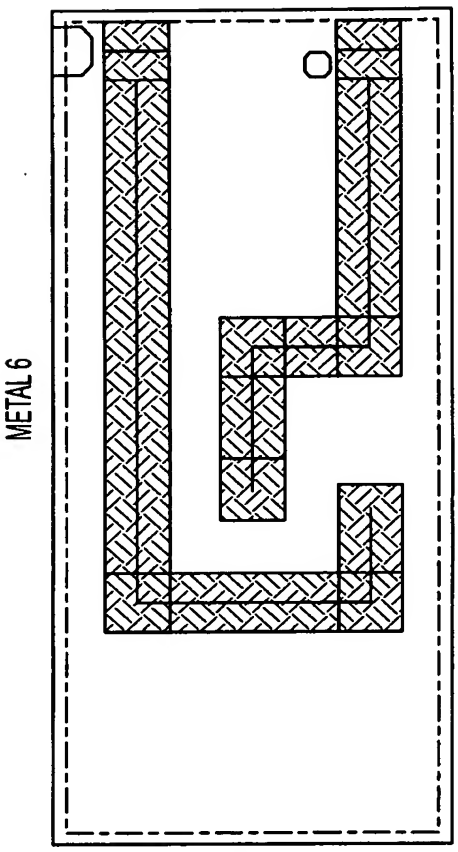


FIG. 21B

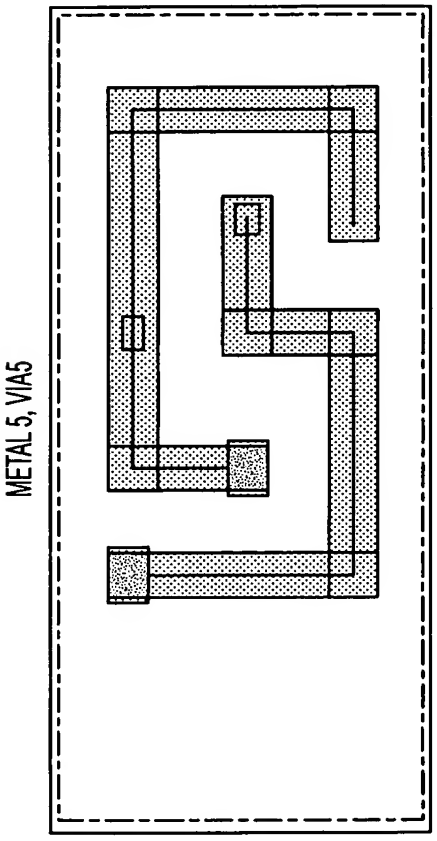


FIG. 21A

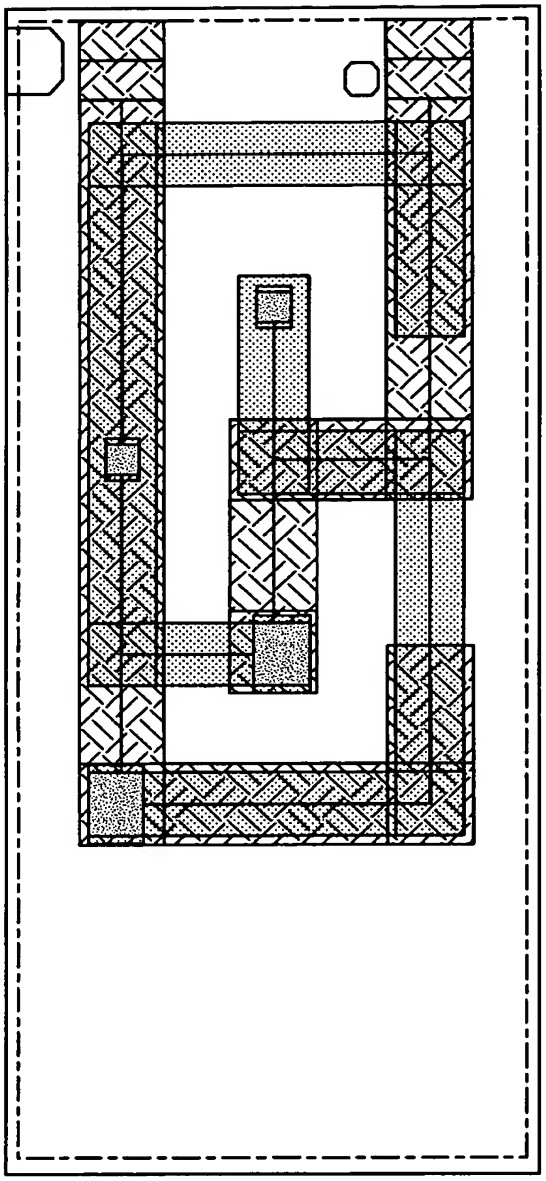


FIG. 21C

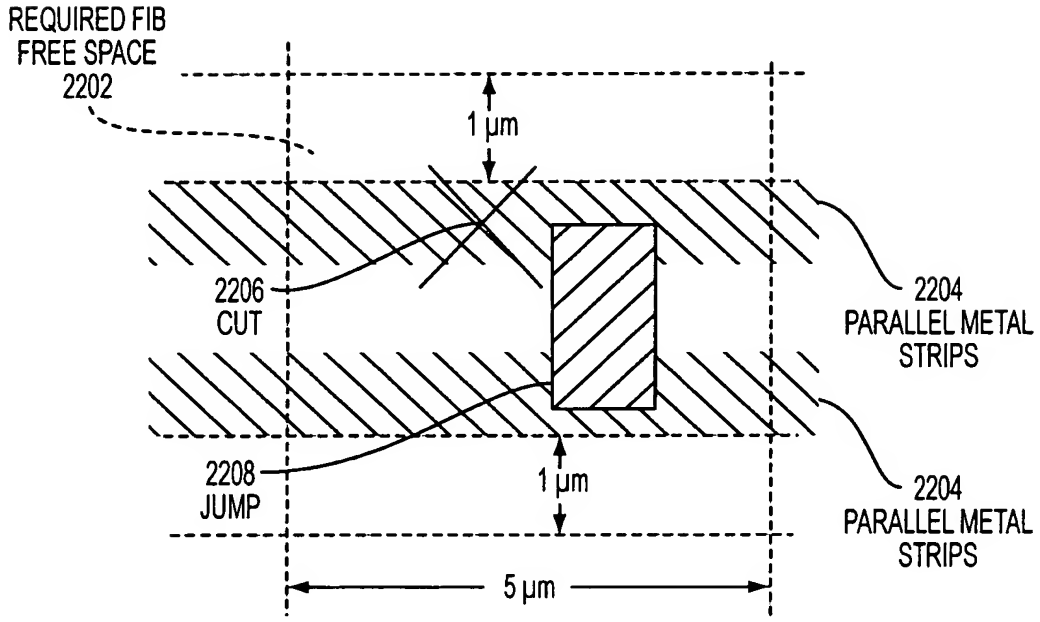

REQUIRED FIB FREE SPACE 2202
1 µm
2206 CUT
2204 PARALLEL METAL STRIPS
2208 JUMP
1 µm
2204 PARALLEL METAL STRIPS
5 µm

FIG. 22

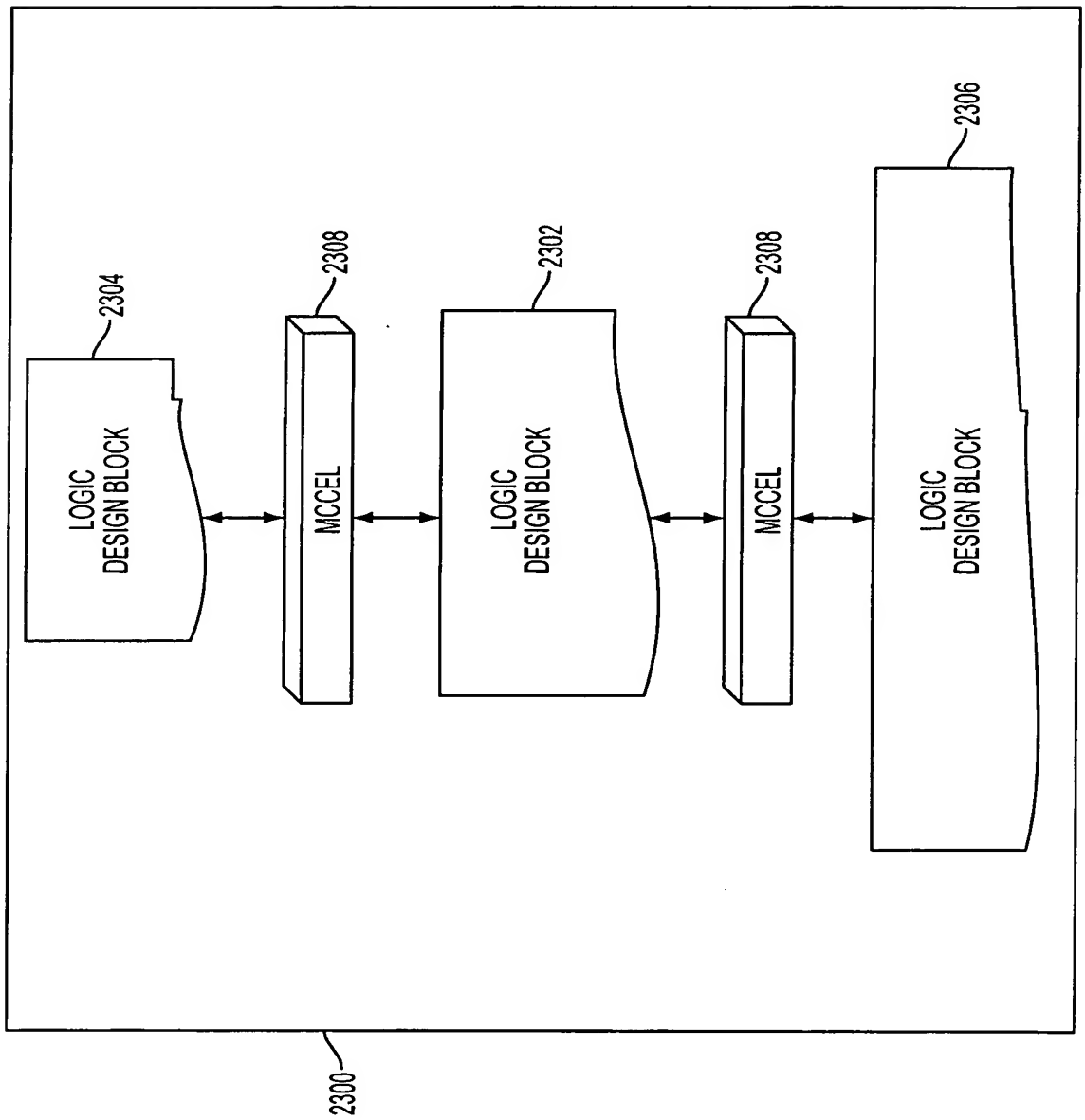

2300
2304
LOGIC DESIGN BLOCK
2308
MCCEL
2302
LOGIC DESIGN BLOCK
2308
MCCEL
2306
LOGIC DESIGN BLOCK

FIG. 23

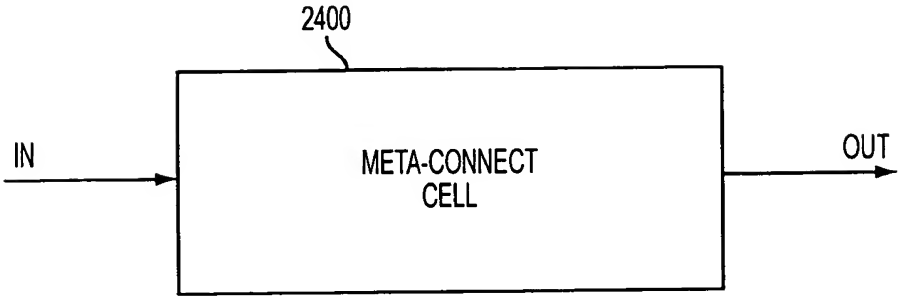


FIG. 24A

OUT	COMMENT
IN	DEFAULT CONNECT AT ANY LAYER
0	TIED TO GND AT ANY LAYER
1	TIED TO VDD AT ANY LAYER

FIG. 24B

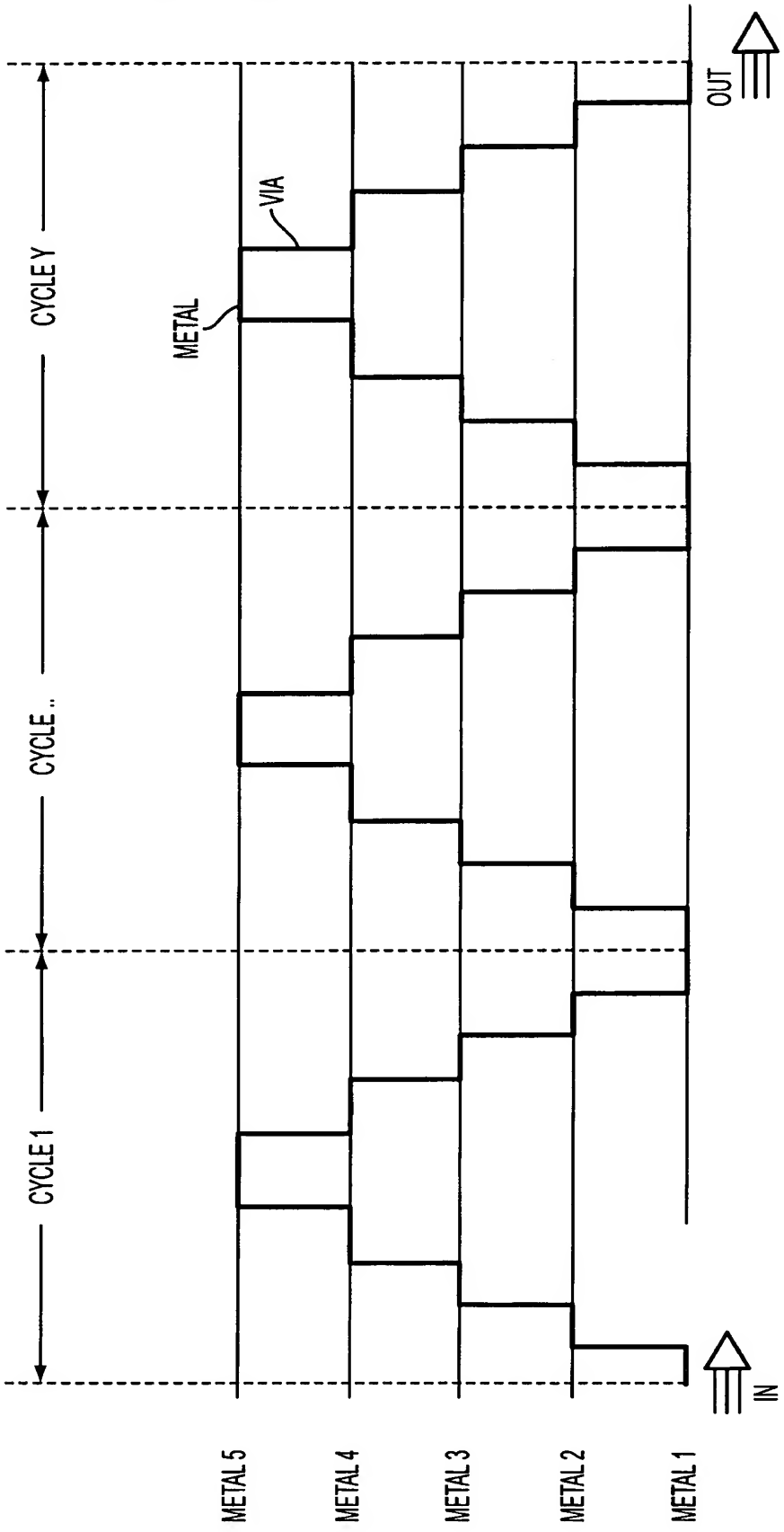

CYCLE Y
CYCLE ..
CYCLE 1
VIA
METAL
OUT
IN
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 25

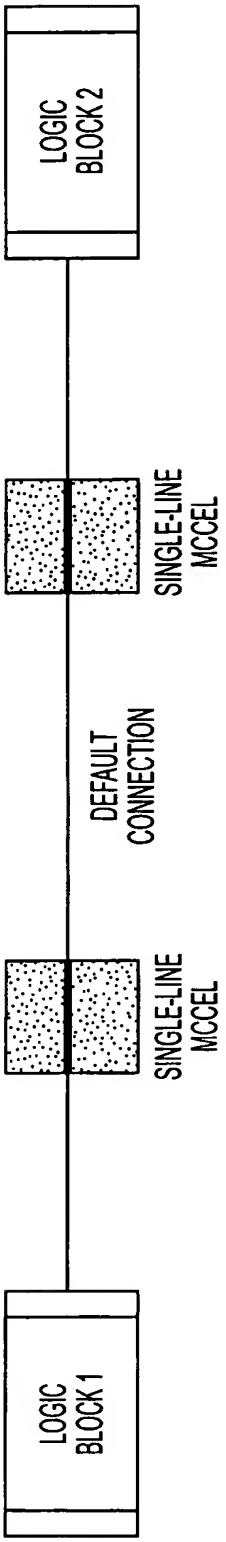


FIG. 26A

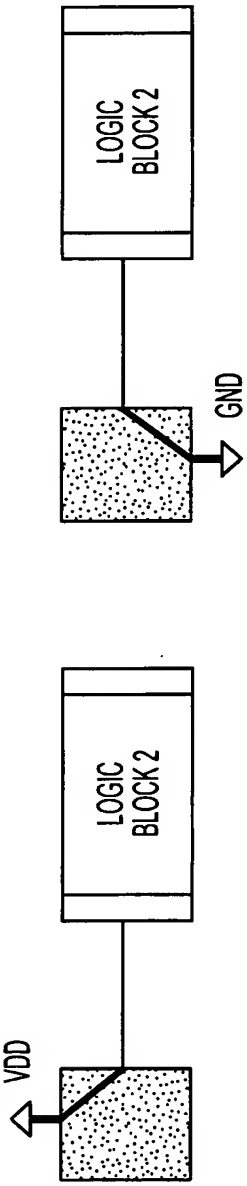


FIG. 26C

FIG. 26B

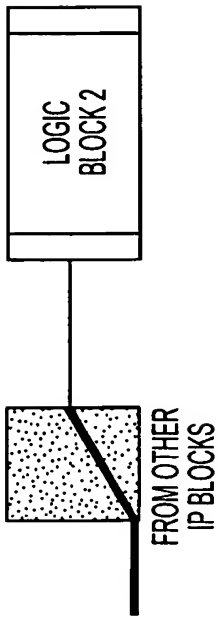


FIG. 26D

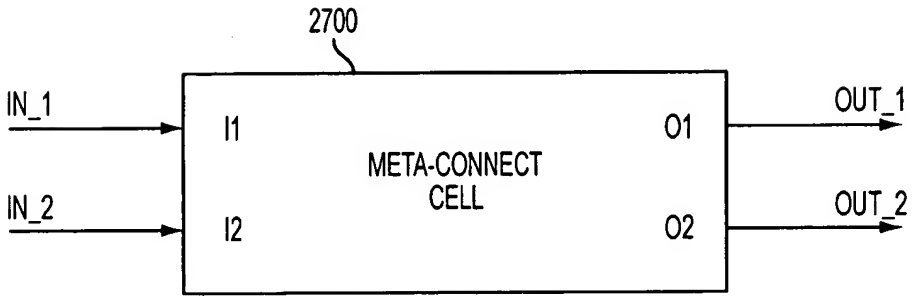


FIG. 27A

TOGGLE	OUT_1	OUT_2	COMMENT
0	IN_1	IN_2	DEFAULT
1	IN_2	IN_1	METAL/VIA CHANGE

FIG. 27B

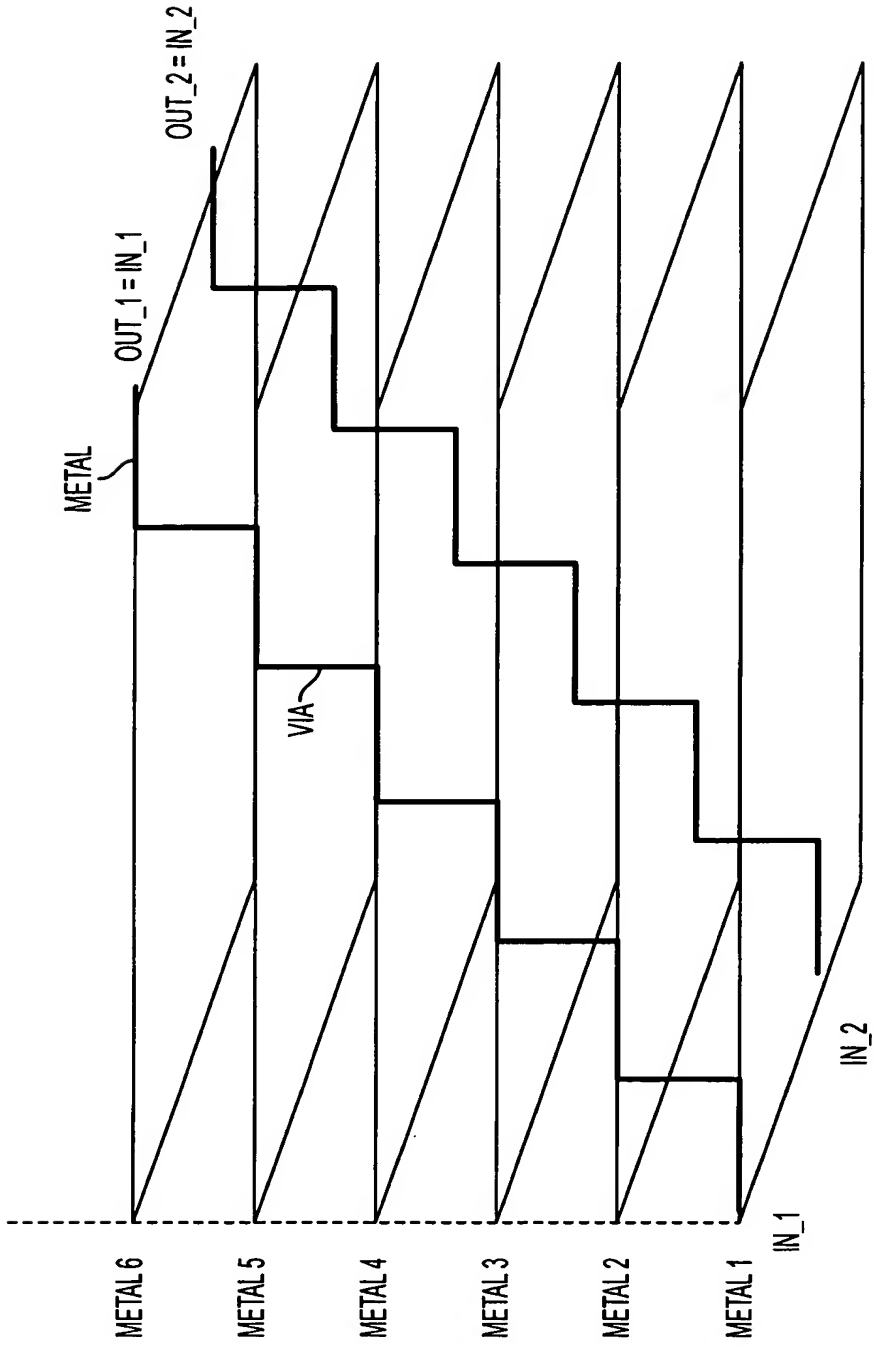

OUT_2 = IN_2
OUT_1 = IN_1
METAL
VIA
IN_2
IN_1
METAL 6
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 28

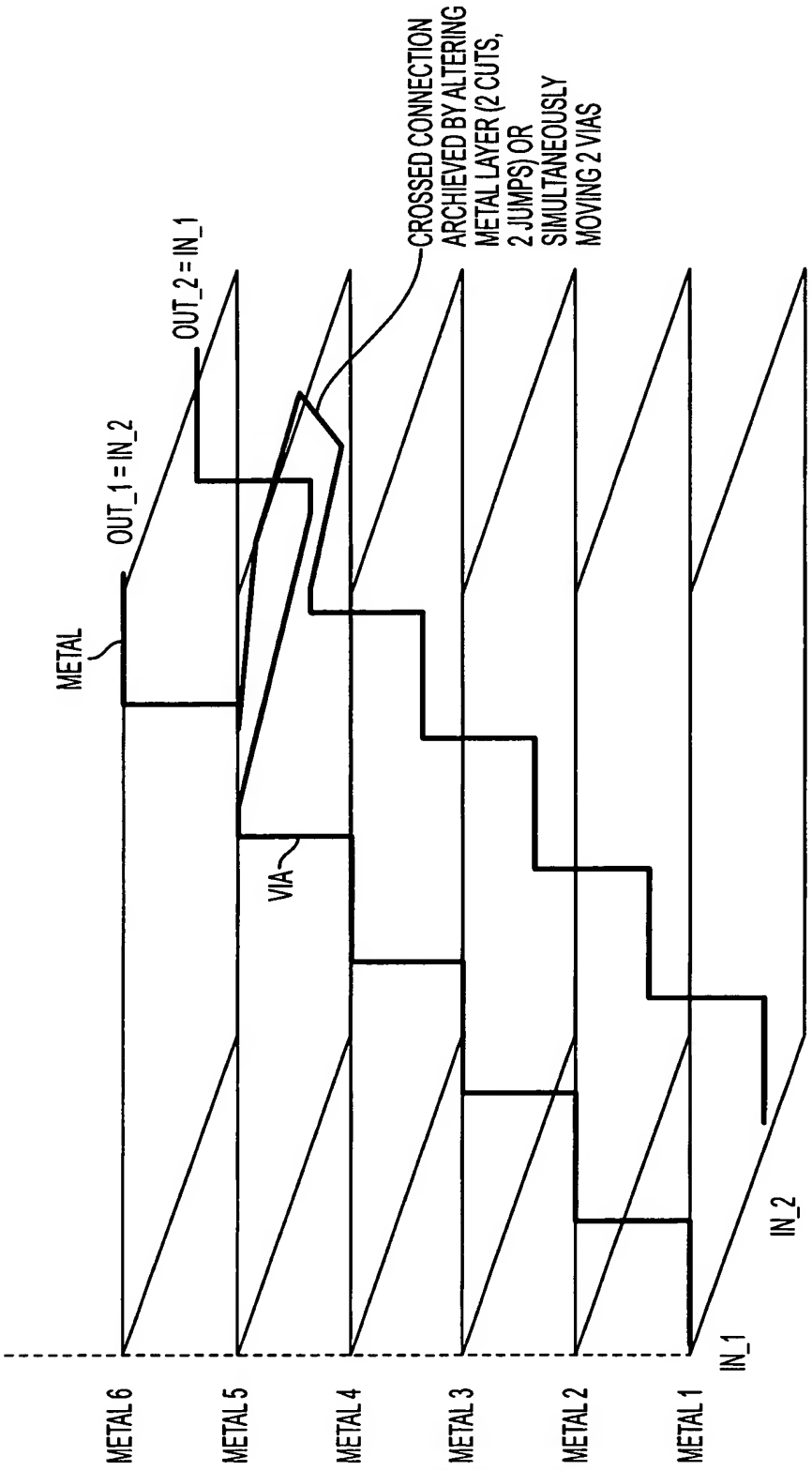

METAL
OUT_1 = IN_2
OUT_2 = IN_1
CROSSED CONNECTION ARCHIEVED BY ALTERING METAL LAYER (2 CUTS, 2 JUMPS) OR SIMULTANEOUSLY MOVING 2 VIAS
VIA
IN_2
IN_1
METAL 6
METAL 5
METAL 4
METAL 3
METAL 2
METAL 1

FIG. 29

OUT_1	OUT_2	COMMENT
OUT	OUT	DEFAULT
OUTB	OUT	METAL/VIA CHANGE

FIG. 30B

OUT 1	OUT2	COMMENT
Q	QB	DEFAULT
QB	Q	METAL/VIA CHANGE

FIG. 30D

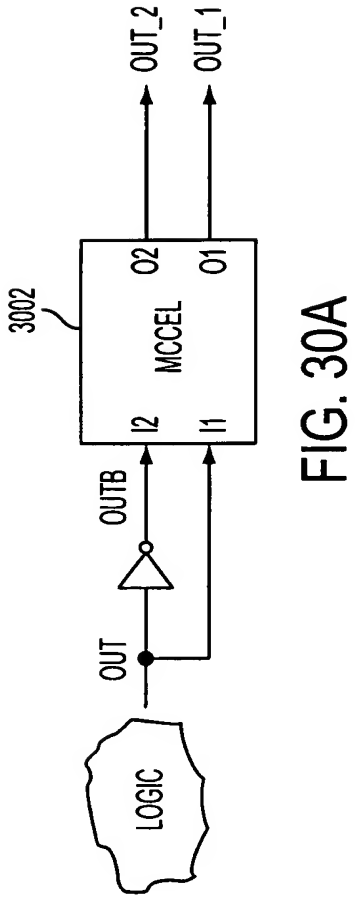


FIG. 30A

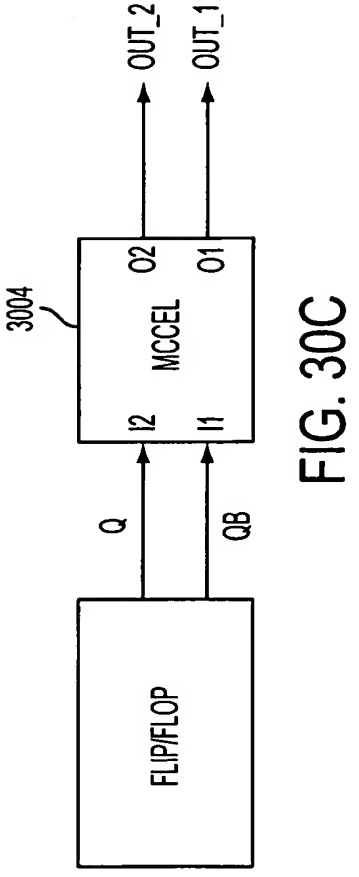


FIG. 30C

OUT_1	OUT_2	COMMENT
0	1	DEFAULT
1	0	METAL/VIA CHANGE

FIG. 31B

OUT_1	OUT_2	COMMENT
WEAK '0'	WEAK '1'	DEFAULT (In_1 & In_2 FLOATING)
WEAK '1'	WEAK '0'	METAL/VIA CHANGE (In_1 & In_2 FLOATING)
in_1	in_2	DEFAULT (In_1 & In_2 DRIVEN)
in_2	in_1	METAL/VIA CHANGE (In_1 & In_2 DRIVEN)

FIG. 31D

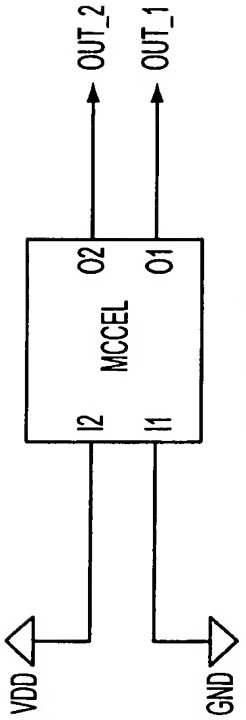


FIG. 31A

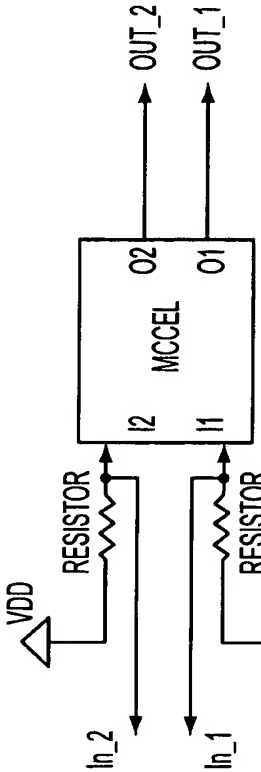


FIG. 31C

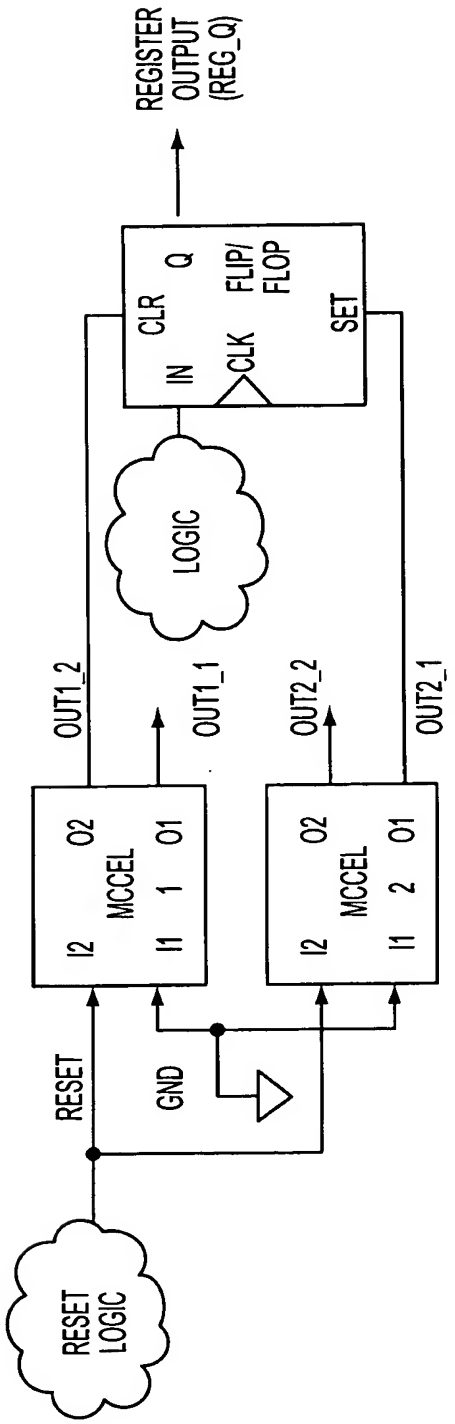


FIG. 32A

RESET	MCCEL1	MCCEL2	REG_Q
0	0	0	Q
0	0	1	Q
0	1	0	Q
0	1	1	Q
1	0	0	0
1	0	1	X
1	1	0	X
1	1	1	1

FIG. 32B

Appl. No. 10/697,289; Filed: Oct 31, 2003
Dkt No. 1875.4360005; Group Unit: 2819
Inventors: CATALASAN et al.
Tel. No.: 202-371-2600
For: Coupling of Signals Between Adjacent Functional Blocks in an Integrated Circuit Chip

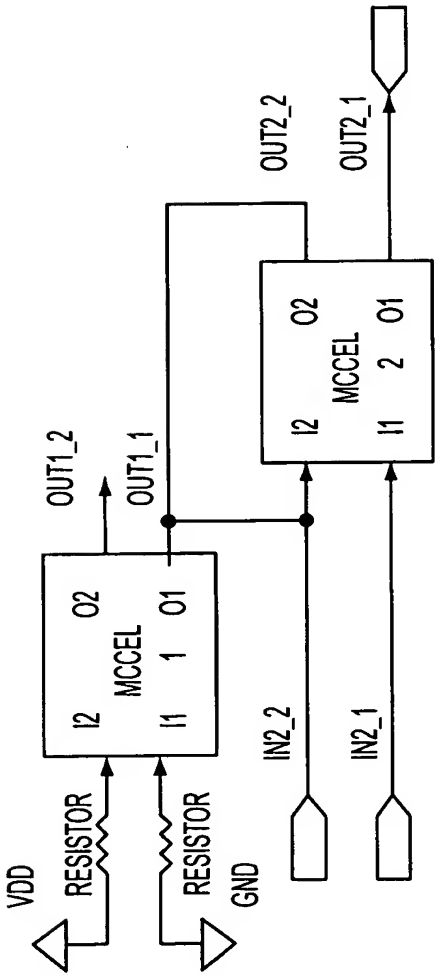


FIG. 33A

MCCEL1	MCCEL2	OUT2_1
0	0	IN2_1 (DEFAULT)
0	1	IN2_1 + IN2_2 + PULL-DOWN
1	0	IN2_1
1	1	IN2_1 + IN2_2 + PULL-UP

FIG. 33B

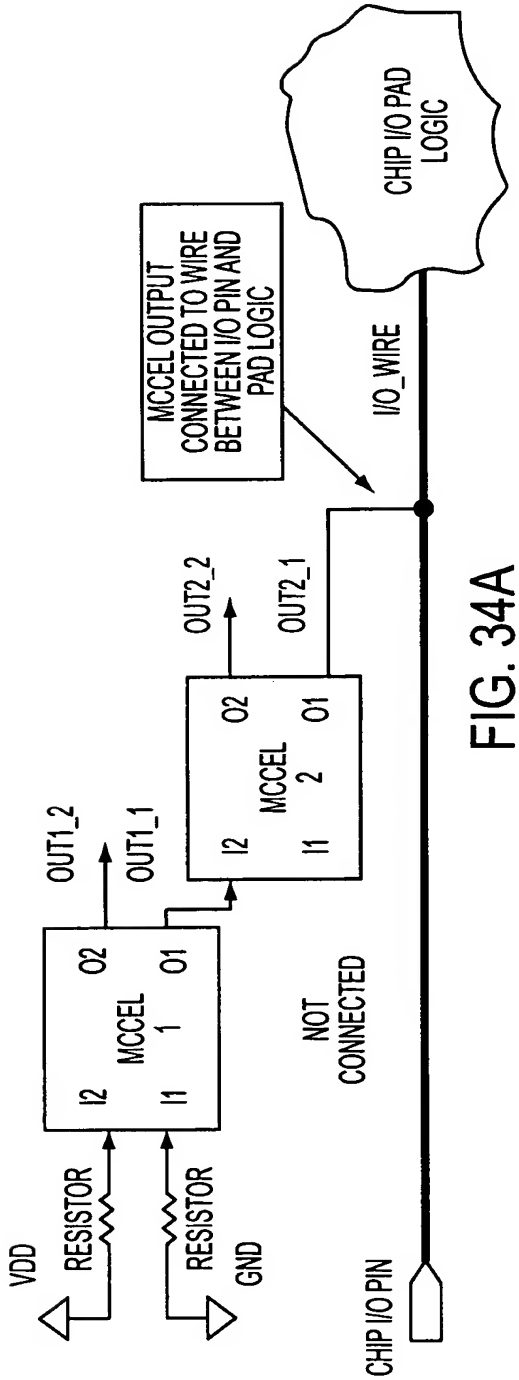


FIG. 34A

MCCEL1	MCCEL2	I/O_PIN
0	0	I/O_WIRE (DEFAULT)
0	1	I/O_WIRE + PULL-DOWN
1	0	I/O_WIRE
1	1	I/O_WIRE + PULL-UP

FIG. 34B

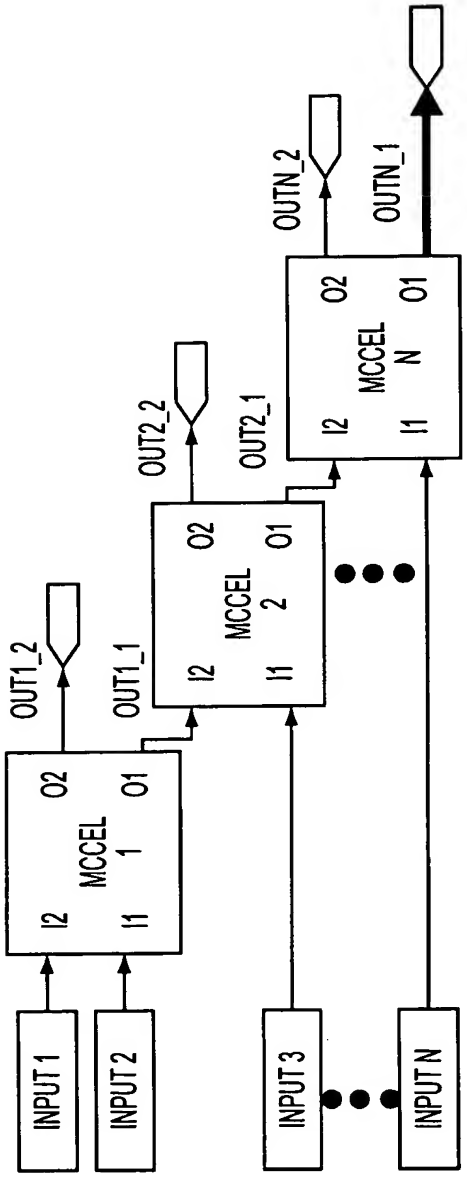

INPUT 1
INPUT 2
INPUT 3
INPUT N
MCCEL 1
MCCEL 2
MCCEL N
I1
I2
O1
O2
OUT1_1
OUT1_2
OUT2_1
OUT2_2
OUTN_1
OUTN_2

FIG. 35

Appl. No. 10/697,289; Filed: Oct 31, 2003
Dkt No. 1875.4360005; Group Unit: 2819
Inventors: CATALASAN et al.
Tel. No.: 202-371-2600
For: Coupling of Signals Between Adjacent Functional Blocks in an Integrated Circuit Chip

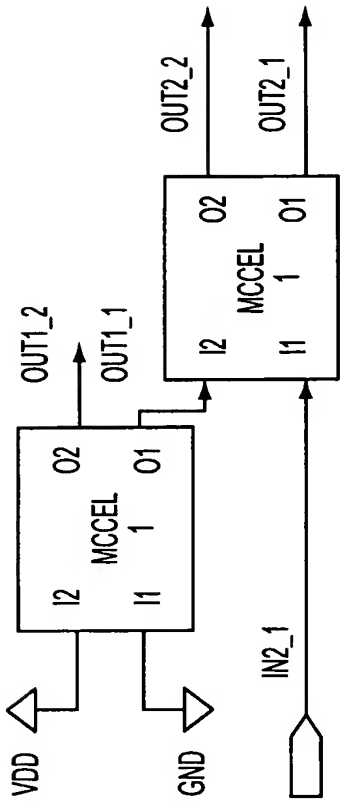


FIG. 36A

MCCEL1	MCCEL1	OUT2_1	OUT2_2
0	0	IN2_1 (DEFAULT)	0 (DEFAULT)
0	1	0	IN2_1
1	0	IN2_1	1
1	1	1	IN2_1

FIG. 36B

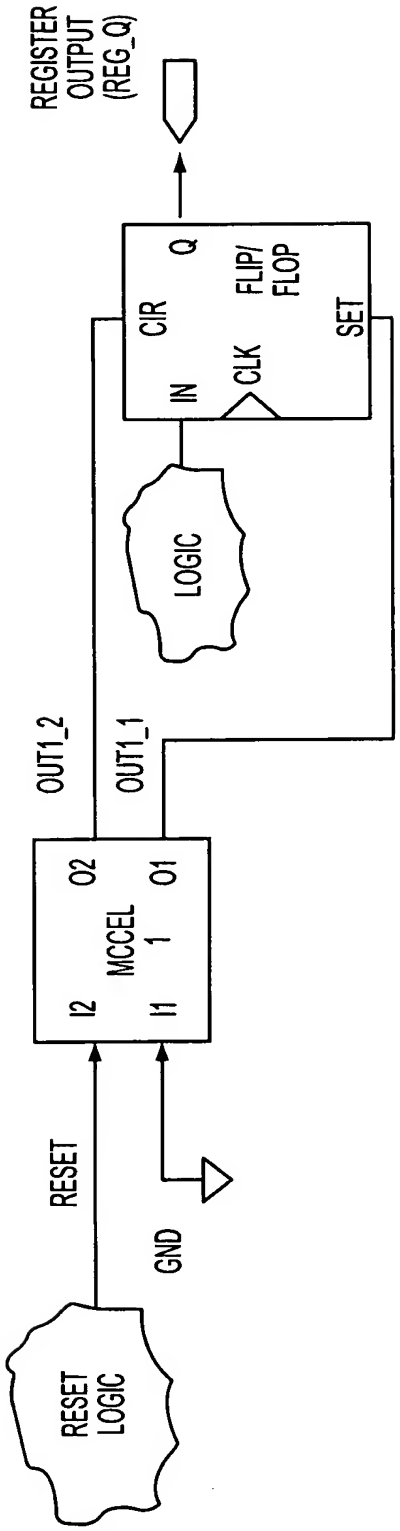


FIG. 37A

RESET	MCCEL1	REG Q
0	0	Q
0	1	Q
1	0	0
1	1	1

FIG. 37B